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41	KB Connector	SB		83	VRAM (BYPASS) 1/2
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Project Code & Schematics Subject:	M930 Main Board	PCB P/N:	(IRIS) (Hannstar)
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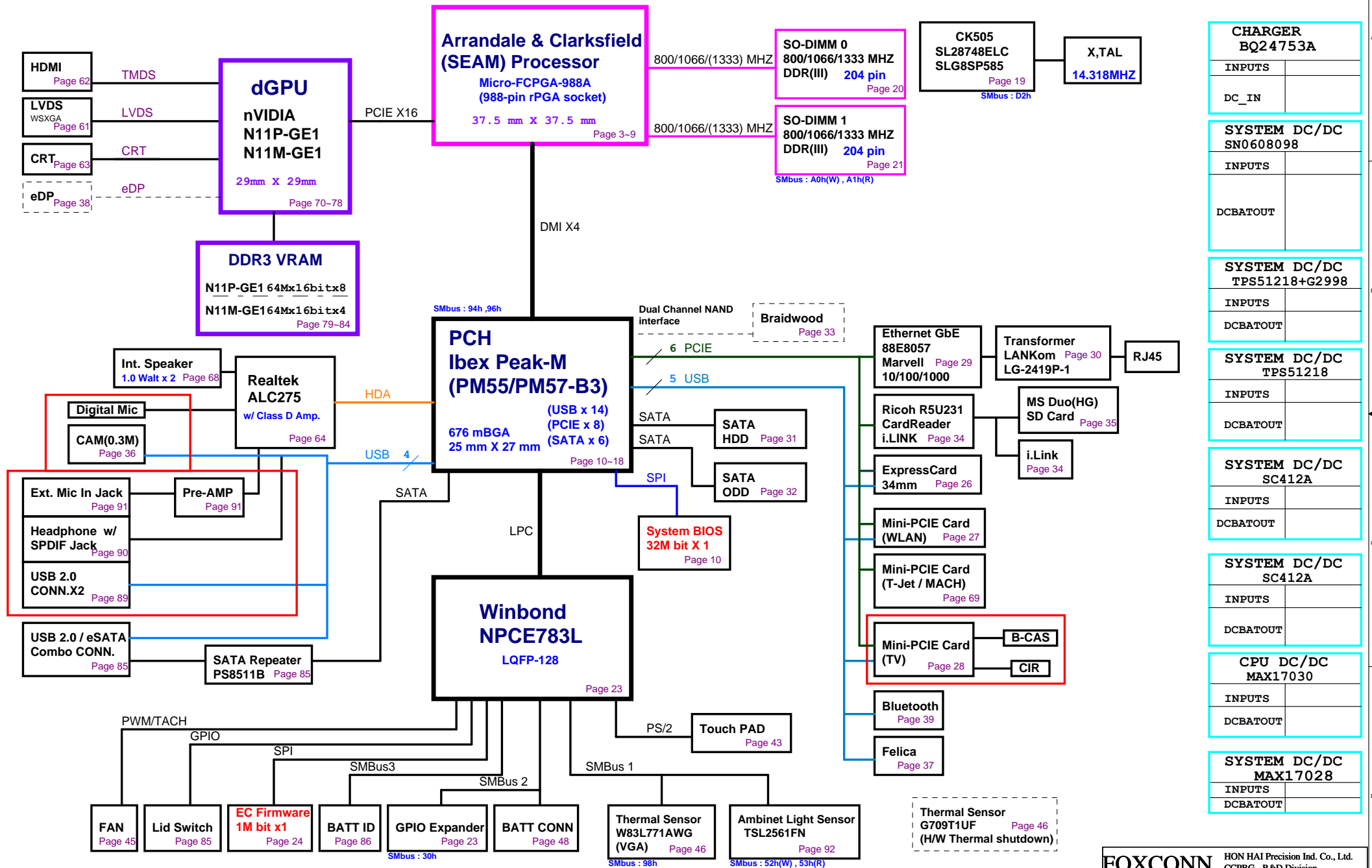
M930 BOM Control Table								
VALUE Head	CFD+PM55 N11P 1GVRAM-H	CFD+PM55 N11P 1GVRAM-S	CFD+PM55 N11M 512MVRAM-H	CFD+PM55 N11M 512MVRAM-S	ARD+SSKU N11P 1GVRAM-H	ARD+SSKU N11P 1GVRAM-S	ARD+SSKU N11M 512MVRAM-H	ARD+SSKU N11M 512MVRAM-S
CF_	Stuff	Stuff	Stuff	Stuff	Dummy	Dummy	Dummy	Dummy
AR_	Dummy	Dummy	Dummy	Dummy	Stuff	Stuff	Stuff	Stuff
NV_	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
NP_	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy
NM_	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff
NVH_	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy
NVS_	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff
NC_	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy

85	LID Switch/eSATA COMBO	SB
86	Identify IC	SB
87	HOLE & AMI LABEL	SB
88	USB & AUDIO Conn.	SB
89	USB Port	SB
90	HP Jack (S/PDIF)	SB
91	Ext MIC Jack	SB
92	Function SW & ALS	SB

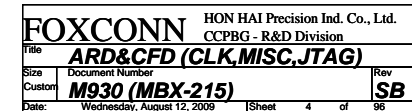
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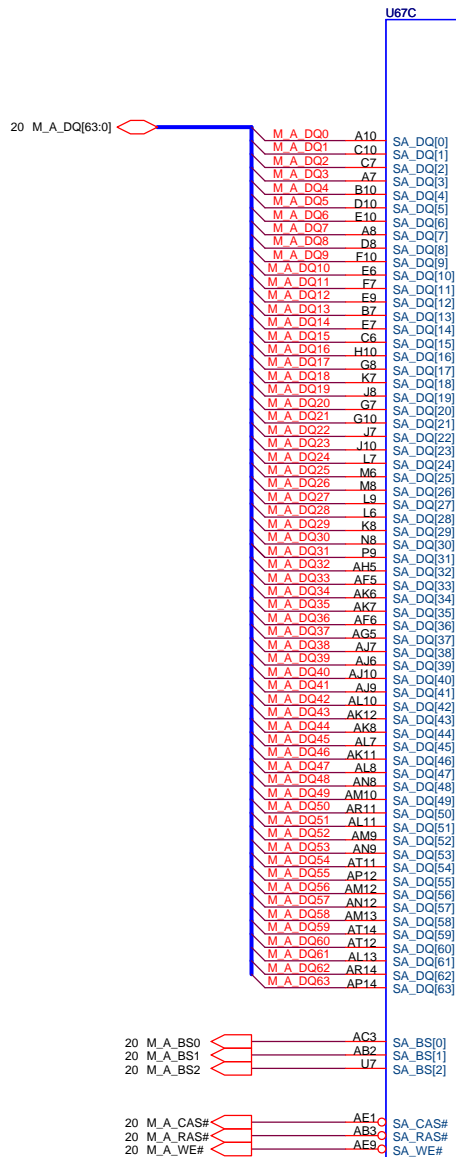
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Index Page		
Size	Document Number		
Custom	M930 (MBX-215)		Rev SB
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M930 (IRX-5100) Calpella Platform+ nVIDIA N11P/M Discrete Graphic



For Disable Auburndale Graphic 7/24 [DVT] Change to Array for C/D
 DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on
 Arrandale directly if motherboard only supports discrete graphics.

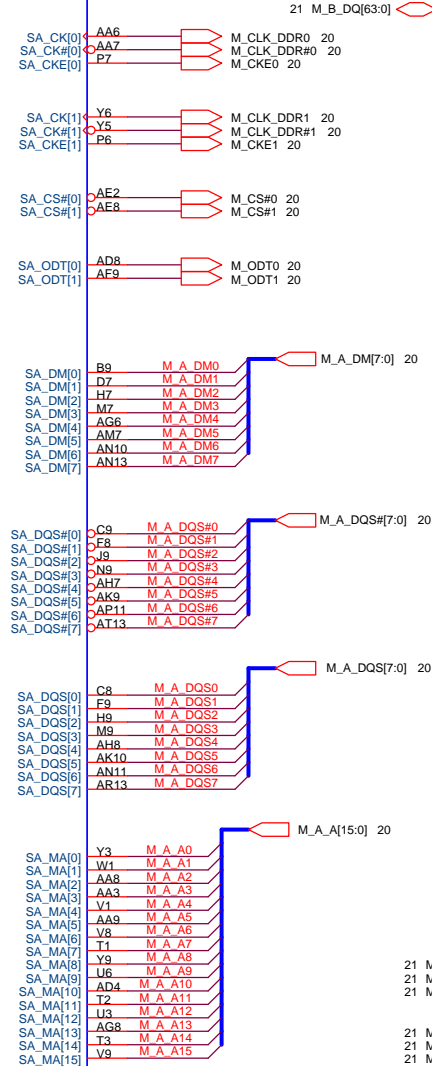




DDR SYSTEM MEMORY A

SOCKET_988P
FOX_PZ98827-364A-01F

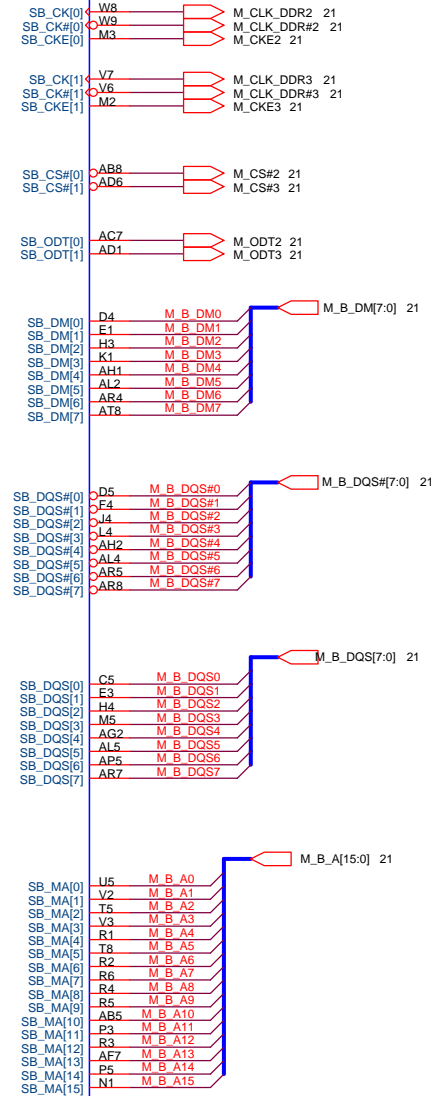
7/13 [DVT] Change to 988A socket.



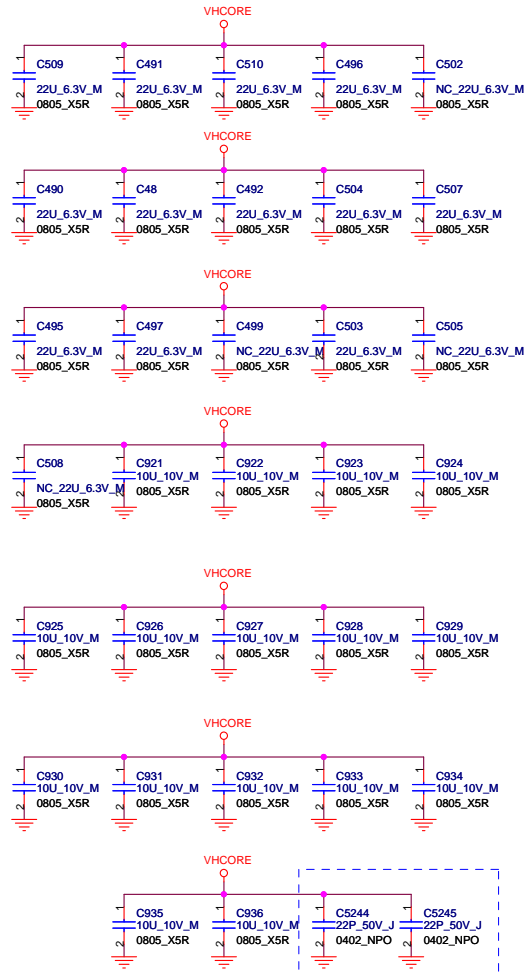
DDR SYSTEM MEMORY - B

SOCKET_988P
FOX_PZ98827-364A-01F

7/13 [DVT] Change to 988A socket.



52A (CFD SV)



For RF Noise

VHOCORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

SOCKET_988P
FOX_P298827-364A-01F

7/13 [DVT] Change to 988A socket.

1.1V RAIL POWER

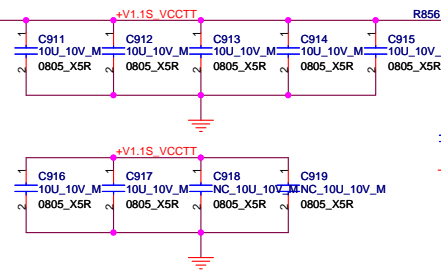
CPU CORE SUPPLY

CPU VIDS

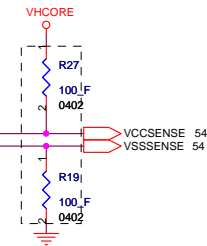
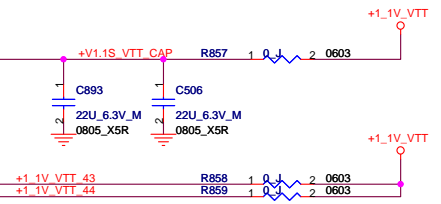
SENSE LINES



18A(CFD SV) (VTT)

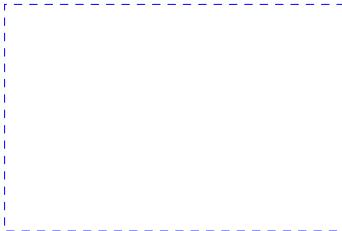


18A(CFD SV) (VTT)



For Disable Auburndale Graphic
VAXG SENSE and VSSAXG SENSE on Arrandale can be left as no connect.
For Disable Auburndale Graphic
In addition, FDI_RXN [7:0] and FDI_RXP [7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The
FDI_IMON, FDI_FSYN[0], FDI_FSYN[1], FDI_LSYN[0], FDI_LSYN[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-k Ω \pm 5% resistors).

For Disable Auburndale Graphic
VAXG should be connected to GND when disable iGPU.

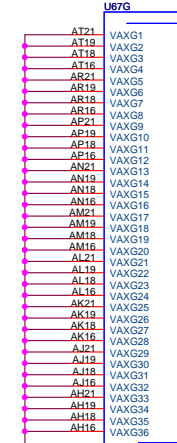
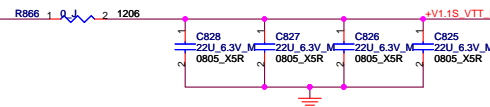


7/8 [DVT] Delete iGPU, Short to GND.

18A(CFD SV) (VTT)



+1.1V_VTT



GRAPHICS

SENSE LINES

GRAPHICS VIDS

POWER

FDI

PEG & DMI

DDR3 - 1.5V RAILS

1.1V

1.8V

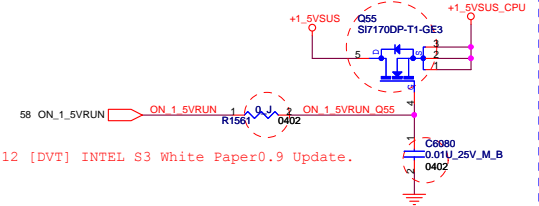
SOCKET_988P
FOX_PZ98827-364A-01F

7/13 [DVT] Change to 988A socket.

7/8 [DVT] Delete iGPU,
Leave to NC.

8/12 [DVT] INTEL White Paper0.9 Check List Request of Q55

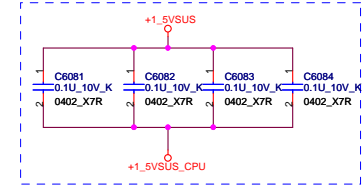
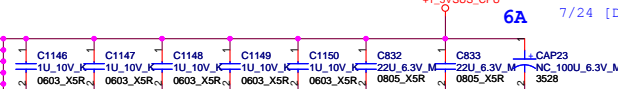
6A



8/12 [DVT] INTEL S3 White Paper0.9 Update.

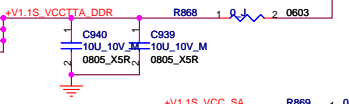
7/24 [DVT] INTEL S3 Power Reduction Solution.

6A

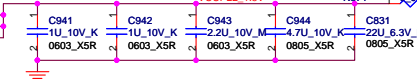


18A(CFD SV) (VTT)

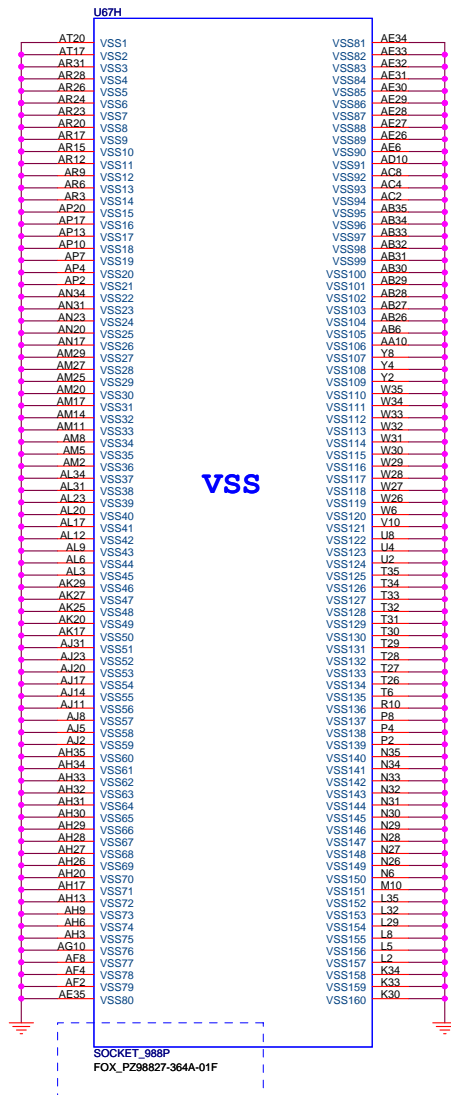
+1.1V_VTT



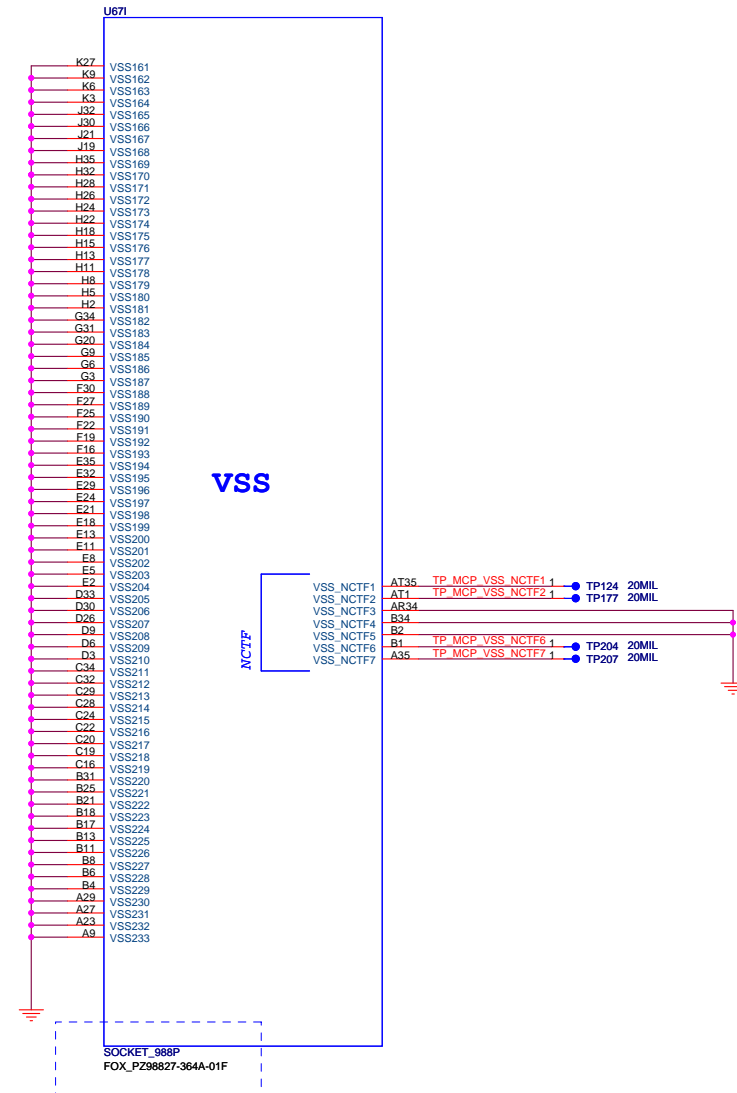
600mA



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ARD&CFD (GRAPHICS POWER)		
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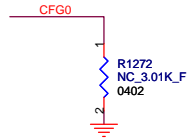


7/13 [DVT] Change to 988A socket.

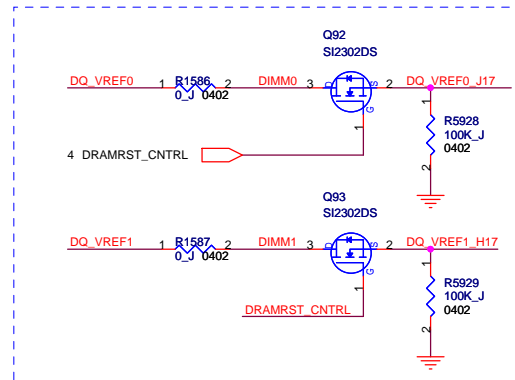
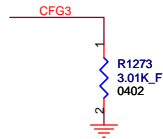


7/13 [DVT] Change to 988A socket.

PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable

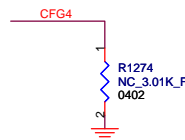


CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 -> 0 , 14 -> 1 , ...



7/24 [DVT] INTEL S3 Power Reduction Solution.

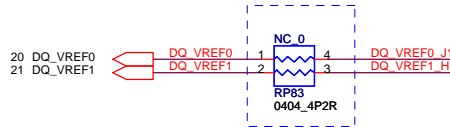
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port
attached to Embedded Display Port
0 : Enable ; An external Display Port device
is connected to the Embedded Display Port



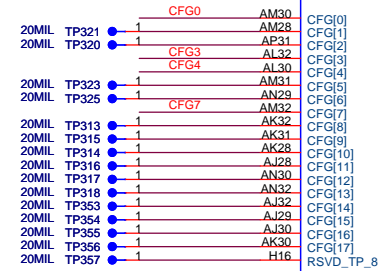
2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

Place RP83 Close to So-DIMM Slot



7/8 [DVT] Support M1/M3 Common Motherboard Design



U67E

RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14

CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
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RSVD15
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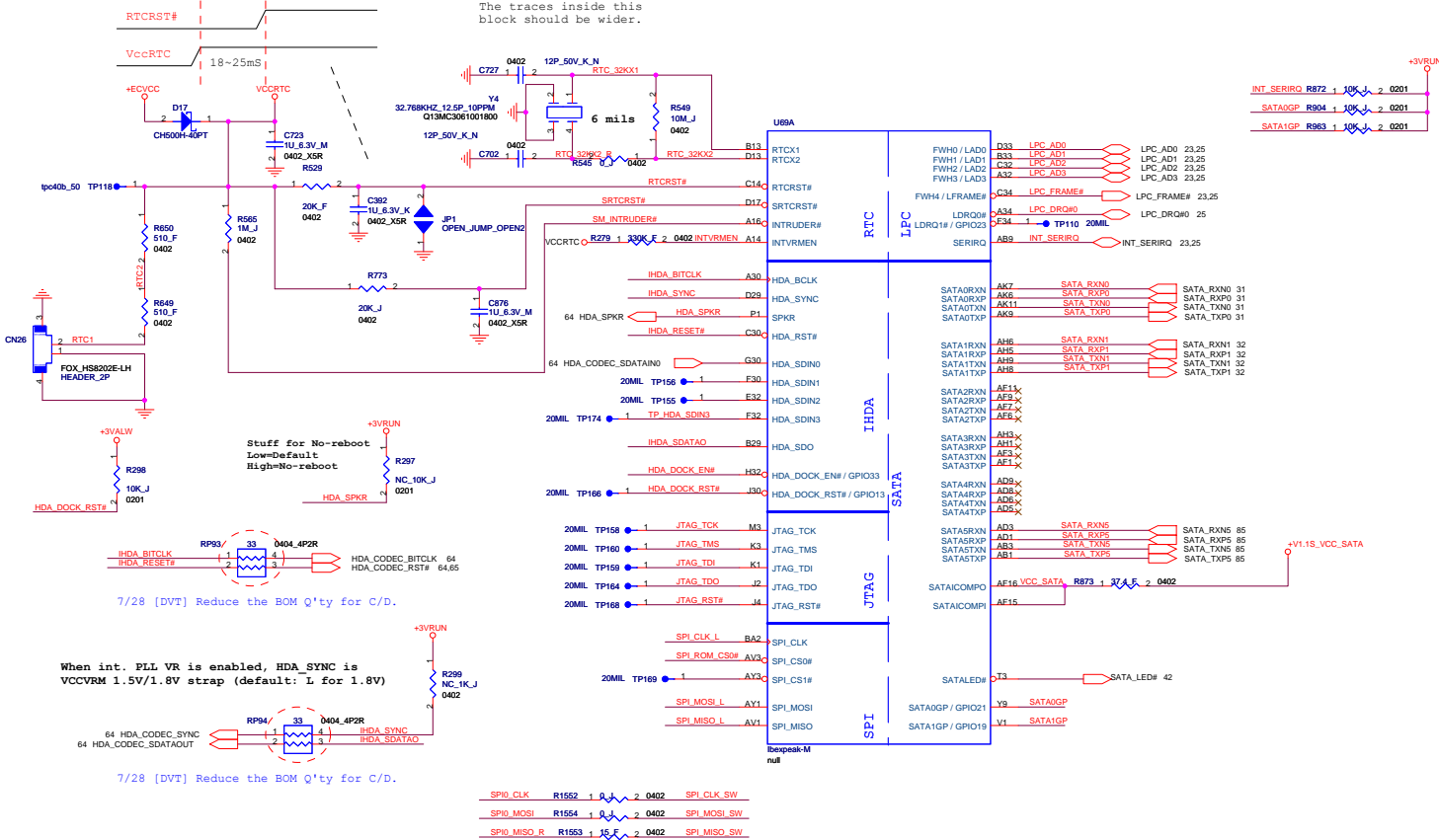
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SOCKET_988P
FOX_PZ98827-364A-01F

7/13 [DVT] Change to 988A socket.

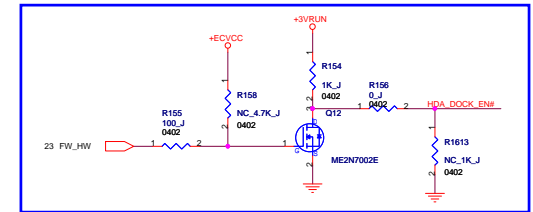
8/3 [DVT] Stuff R1582

The traces inside this block should be wider.

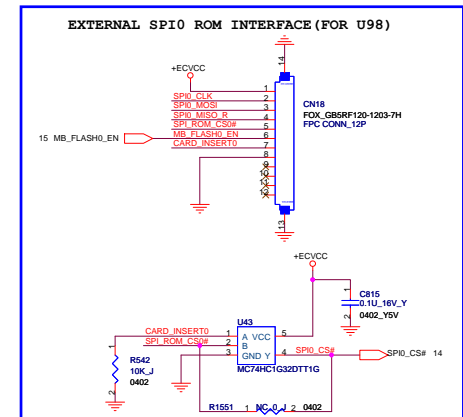


[HDA_DOCK_EN#/GPIO33]

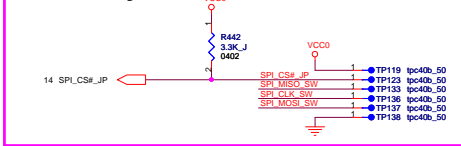
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) - Security measure defined in the Flash Descriptor will be enabled



For MP, Dummy CN18, C815, U43, R542, Stuff R1551



For SW Debug

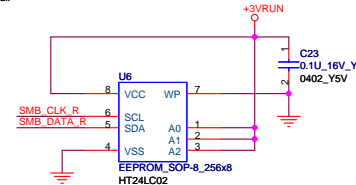
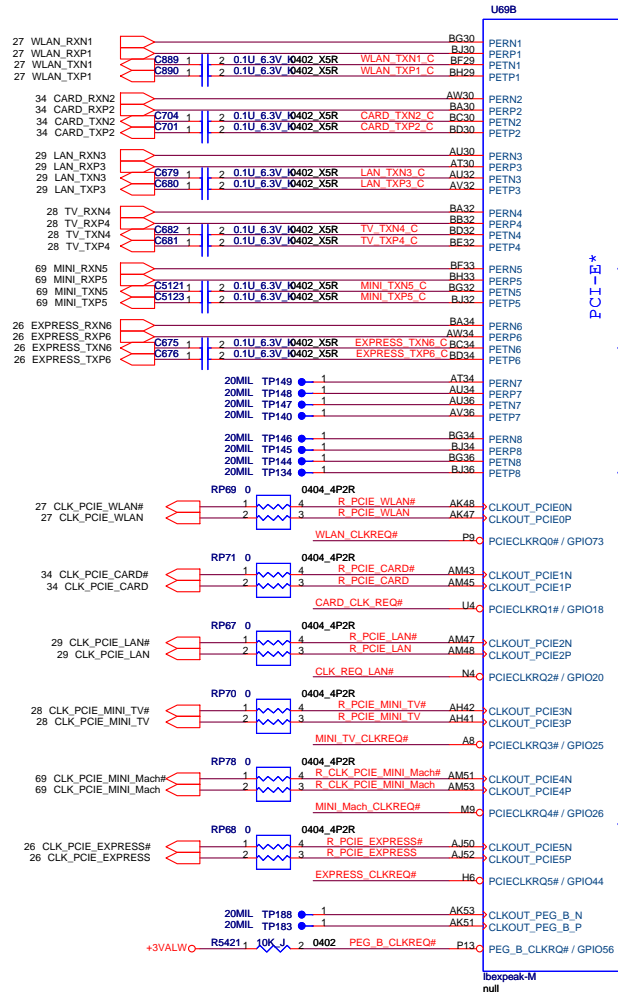
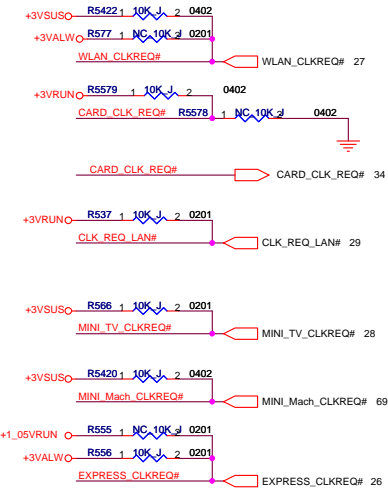


Strap for PCH SPI Program (SW5)	
X	Normal Operation
2 - 3 (ON)	Programming SPI0 (U98)

7/15 [DVT] Change U98 to MX25L3205DM2I-12G.

PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	ISDB-T Tuner (JP)
Port5	Mach/Tsubaki
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC



SMBus Address: AEH

SMBALERT# / GPIO11 B9 WAKE_SCI# WAKE_SCI# 23

SMBCLK H14 SMB_CLK_R PCH EEPROM/CKG/DIMM/ExpressCard

SMBDATA C81 SMB_DATA_R

SML0ALERT# / GPIO60 J14 GPIO60

SML0CLK C6 SML0_CLK

SML0DATA G8 SML0_DATA

SML1ALERT# / GPIO74 M14 LPD_SPI_INTR#

SML1CLK / GPIO58 E10 SMB_THRM_CLK SMB_THRM_CLK 23,40,46,64,76

SML1DATA / GPIO75 G12 SMB_THRM_DATA SMB_THRM_DATA 23,40,46,64,76

EC/THM/ALS/dGPU
(SMBus Address: 94h,96h)

CL_CLK1 T13

CL_DATA1 T11

CL_RST1# T9

PEG_A_CLKREQ# / GPIO47 H1 PEG_CLKREQ# PEG_CLKREQ# 70

CLKOUT_PEG_A_N AD43 CLK_PEG# RP89 NV 0 0404_4P2R

CLKOUT_PEG_A_P AD45 CLK_PEG 2 3

CLKOUT_DMI_N AN4 CLK_EXP_N 4

CLKOUT_DMI_P AN2 CLK_EXP_P 4

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1 CLK_DP_N 1 TP89 20MIL

CLKOUT_DP_P / CLKOUT_BCLK1_P AT3 CLK_DP_P 1 TP90 20MIL

CLKIN_DMI_N AW24 CLK_DMI_PCH# 19

CLKIN_DMI_P BA24 CLK_DMI_PCH 19

CLKIN_BCLK_N AP3 CLK_MCH_BCLK# 19

CLKIN_BCLK_P AP1 CLK_MCH_BCLK 19

CLKIN_DOT_96N E18 DREFCLK# 19

CLKIN_DOT_96P E18 DREFCLK 19

CLKIN_SATA_N / CKSSCD_N AH13 CLK_PCIE_SATA# 19

CLKIN_SATA_P / CKSSCD_P AH12 CLK_PCIE_SATA 19

REFCLK14IN P41 REF_14M_PCH 19

CLKIN_PCLOOPBACK J42 CLK_PCL_FB 14

XTAL25_IN AH51 XTAL25_IN

XTAL25_OUT AH53 XTAL25_OUT

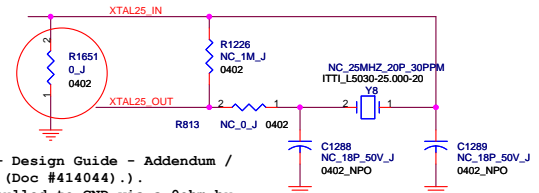
XCLK_RCOMP AF38 XCLK_RCOMP R1225 90.9_F 0402

CLKOUTFLEX0 / GPIO64 T45 CLKOUTLEX0 TP88 20MIL

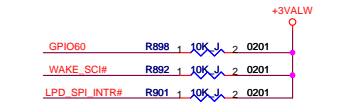
CLKOUTFLEX1 / GPIO65 P43 CLKOUTLEX1 TP91 20MIL

CLKOUTFLEX2 / GPIO66 T42 CLKOUTLEX2 TP93 20MIL

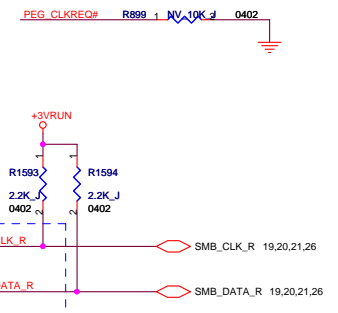
CLKOUTFLEX3 / GPIO67 N50 CLKOUTLEX3 TP101 20MIL



Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).
XTAL_IN should be pulled to GND via a 0ohm by default.
This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

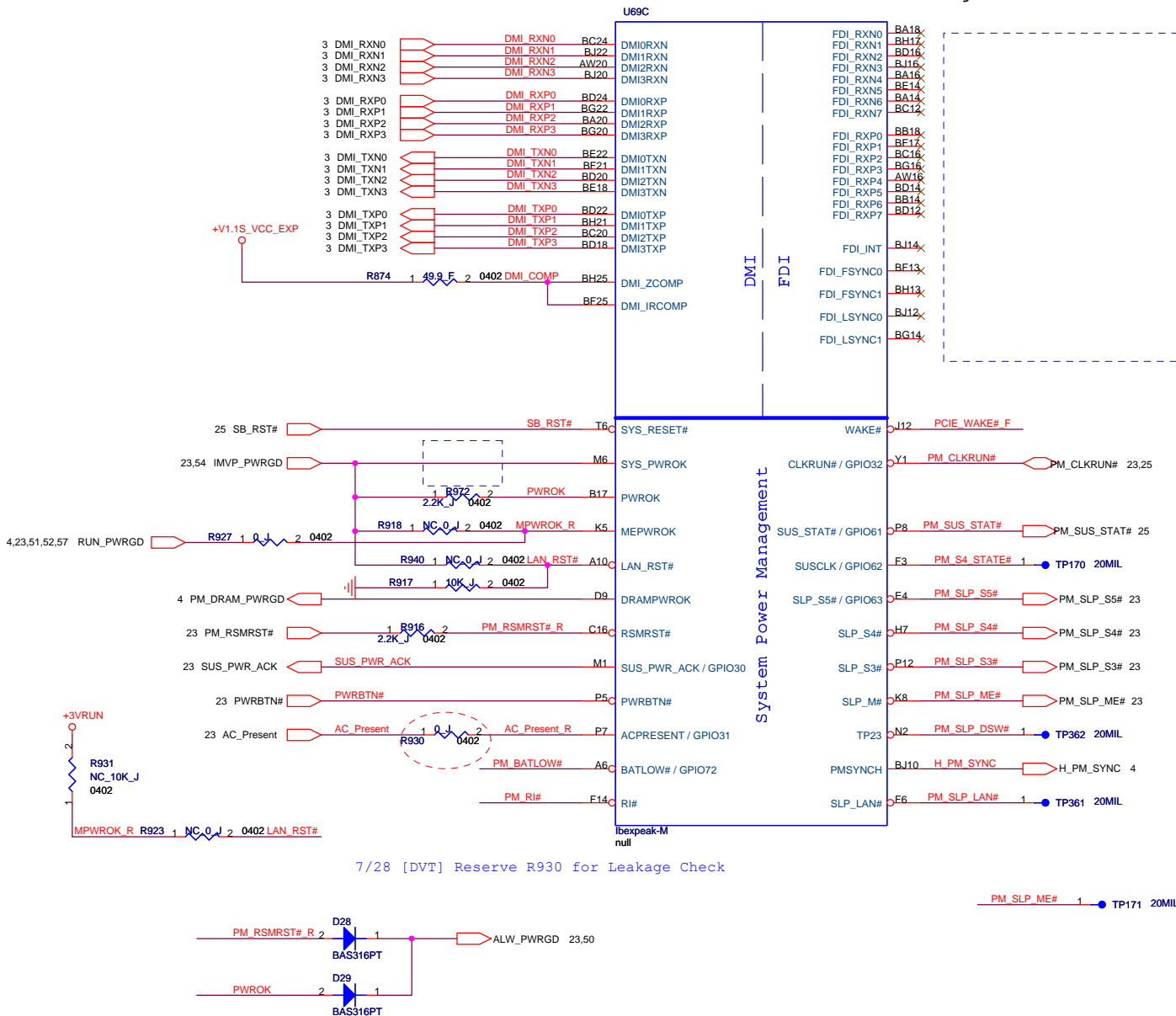


6/24 [DVT] - Change to ALW Power Rail as DG and SCL.



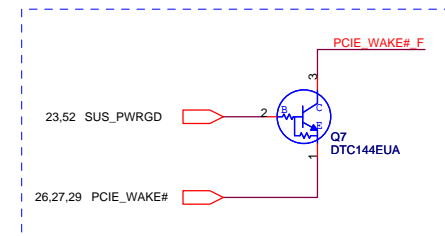
7/8 [DVT] Delete Dummy Parts and Change Net name.

For Disable Auburndale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The
GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-k Ω \pm 5% resistors).

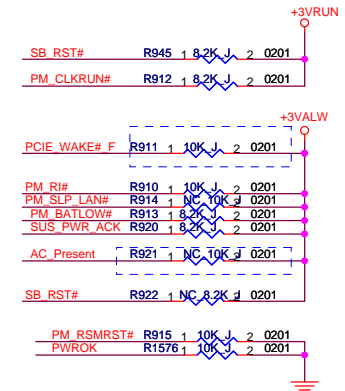


7/8 [DVT] Delete iGPU, Leave NC.

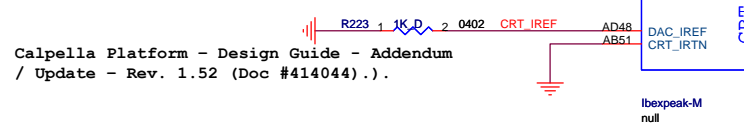
7/31 [DVT] Add the Q7 as MOR request.



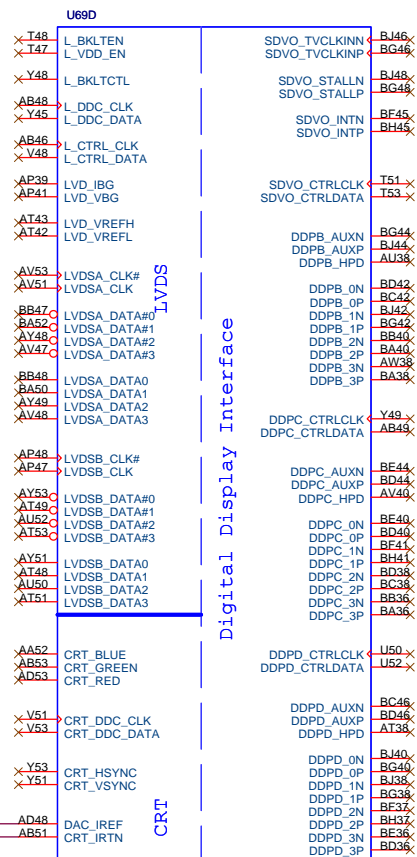
7/24 [DVT] Change R911 to 10Kohm as MOR request.



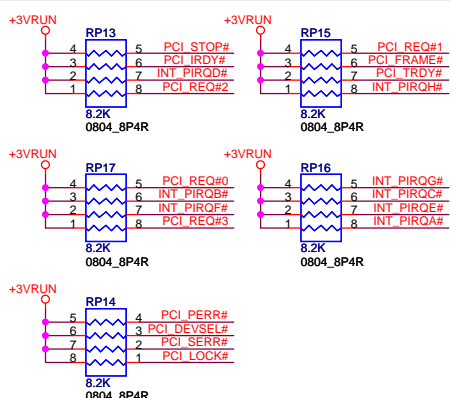
Calpella Platform - Design Guide - Addendum
/ Update - Rev. 1.52 (Doc #414044)..



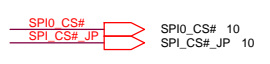
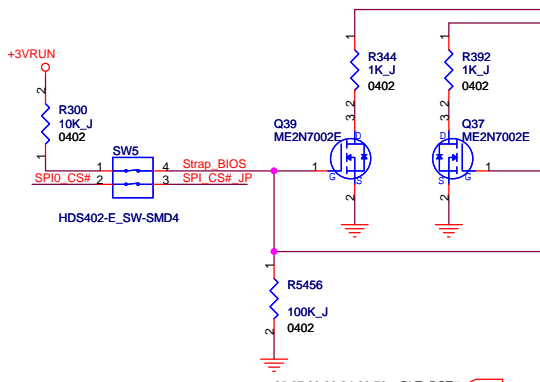
7/8 [DVT] Delete iGPU, Leave NC.



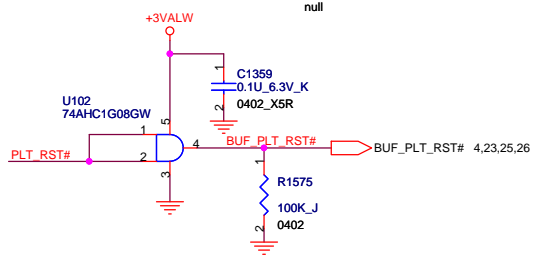
7/8 [DVT] Delete iGPU, Leave NC.



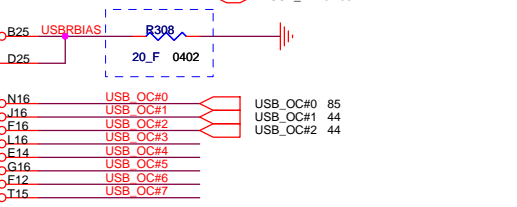
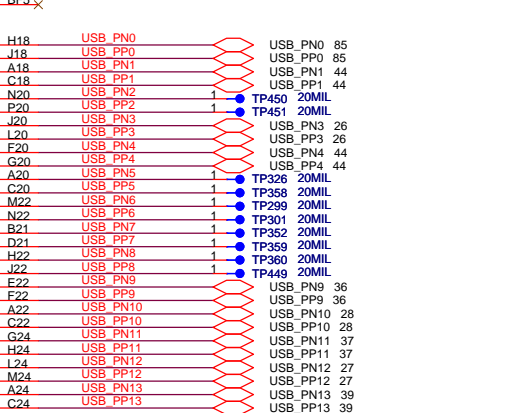
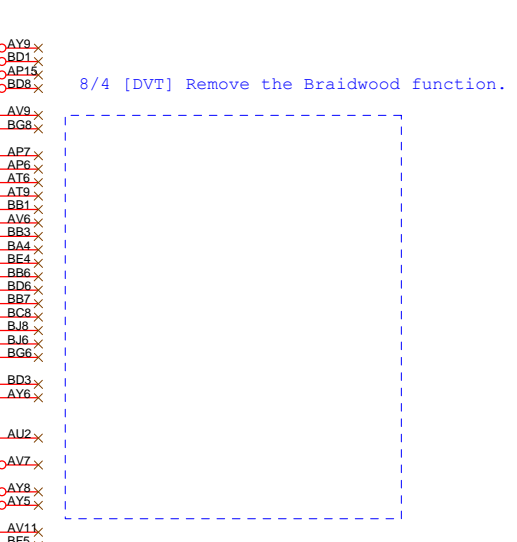
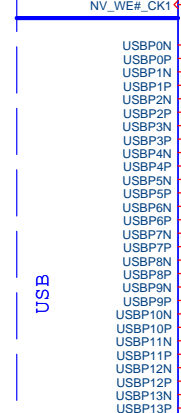
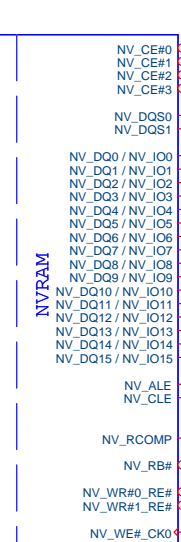
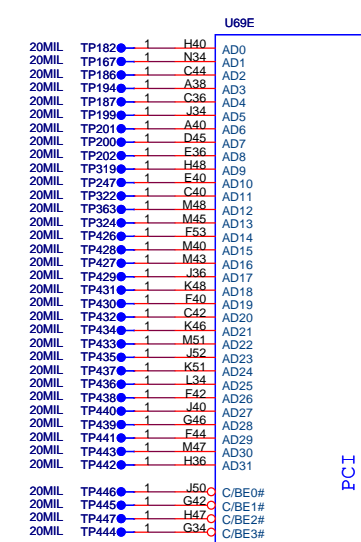
Strap for Boot-BIOS (SW5)		
	GNT1# (Q37)	GNT0# (Q39)
LPC 1-4 (ON)	LOW	LOW
SPI X	Hi	Hi



Strap for PCH SPI Program (SW5)	
X	Normal Operation
2 - 3 (ON)	Programing SPI0 (U98)



Buffer to reduce loading on PLT_RST#.



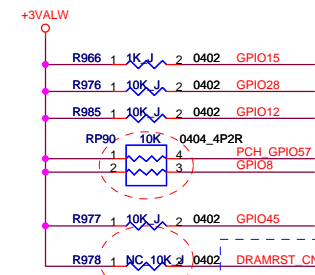
8/4 [DVT] Remove the Braidwood function.

7/8 [DVT] Change value from 22.6ohm to 20ohm.

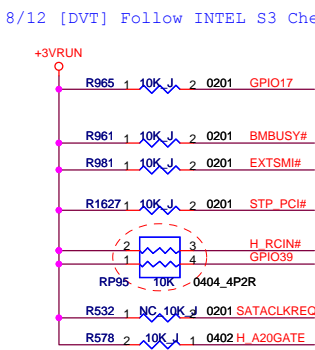
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High , Stuff R1616

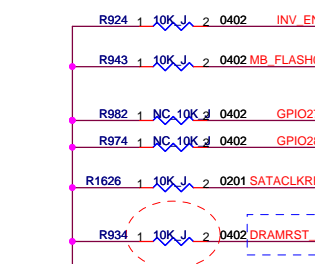
USB PORT	Function
PORT-0	On Board Port
PORT-1	External Port
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	IR Receiver (JP)
PORT-11	Felica
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth



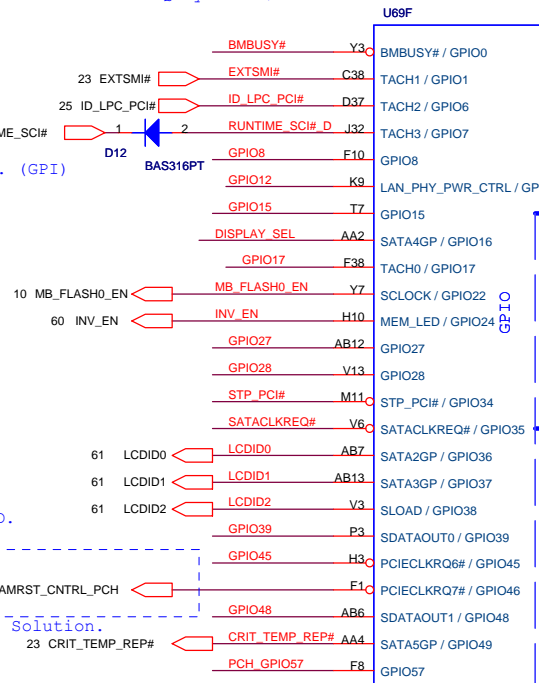
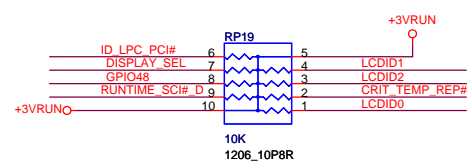
7/28 [DVT] Reduce the BOM Q'ty for C/D.



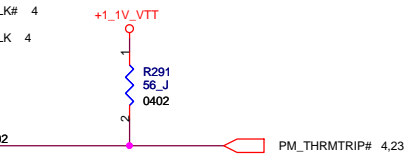
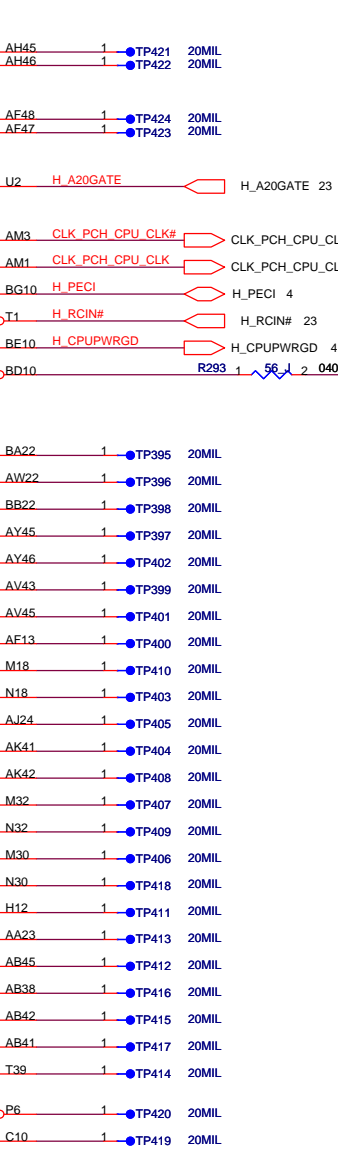
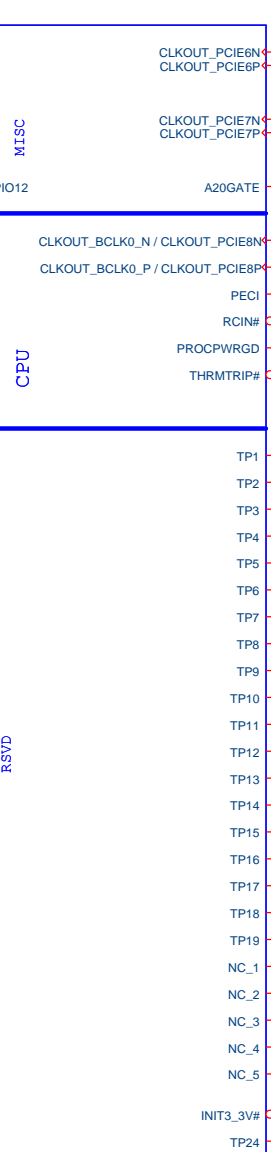
7/28 [DVT] Reduce the BOM Q'ty for C/D.



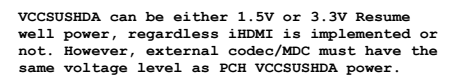
8/12 [DVT] Follow INTEL S3 Check List 0.9. (GPO)



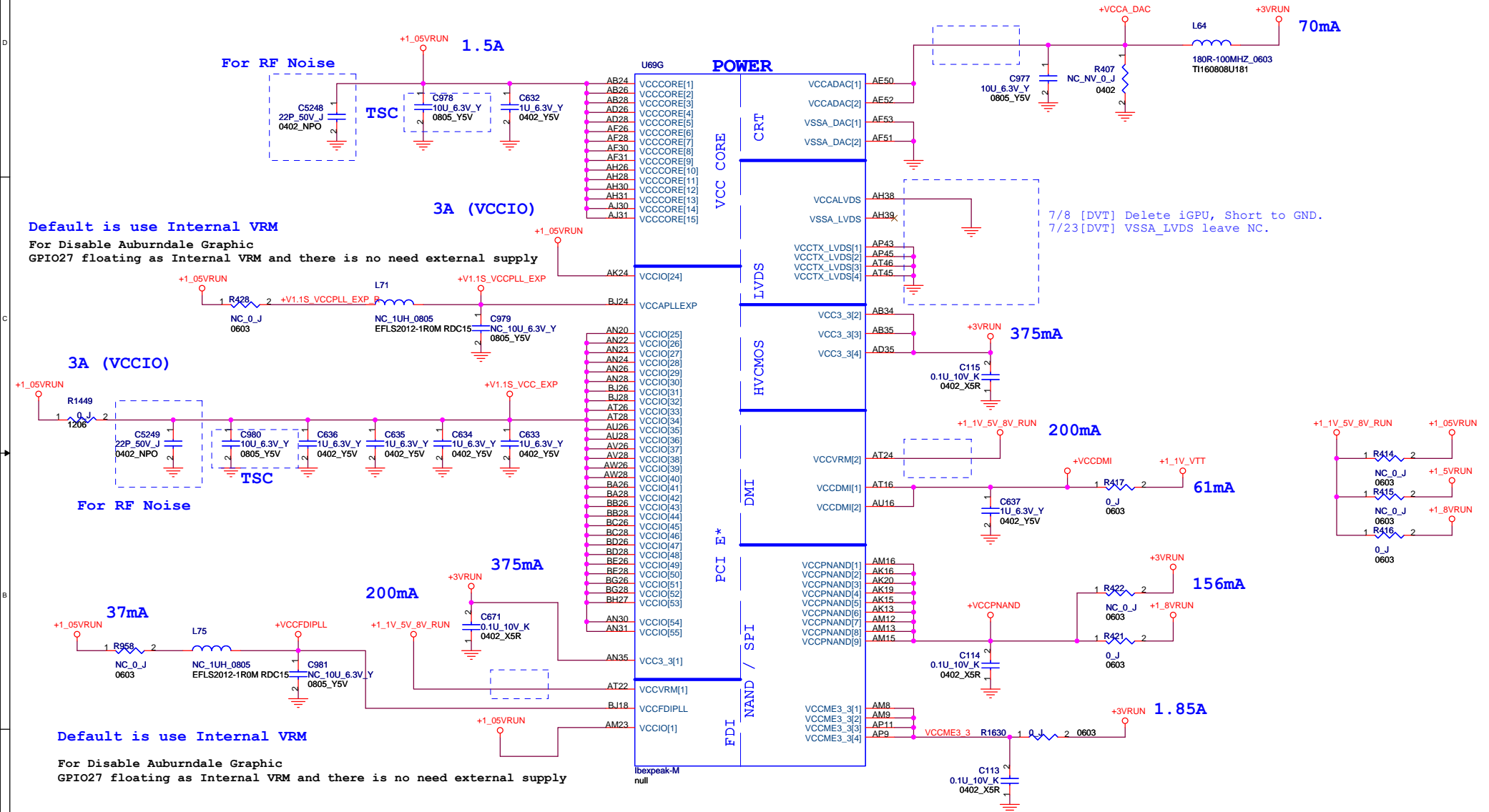
- X A4 VSS_NCTF_1
- X A49 VSS_NCTF_2
- X A5 VSS_NCTF_3
- X A50 VSS_NCTF_4
- X A52 VSS_NCTF_5
- X A53 VSS_NCTF_6
- X B2 VSS_NCTF_7
- X B4 VSS_NCTF_8
- X B52 VSS_NCTF_9
- X B53 VSS_NCTF_10
- X BE1 VSS_NCTF_11
- X BE53 VSS_NCTF_12
- X BF1 VSS_NCTF_13
- X BE53 VSS_NCTF_14
- X BH1 VSS_NCTF_15
- X BH2 VSS_NCTF_16
- X BH52 VSS_NCTF_17
- X BH53 VSS_NCTF_18
- X BJ1 VSS_NCTF_19
- X BJ2 VSS_NCTF_20
- X BJ4 VSS_NCTF_21
- X BJ49 VSS_NCTF_22
- X BJ5 VSS_NCTF_23
- X BJ50 VSS_NCTF_24
- X BJ52 VSS_NCTF_25
- X BJ53 VSS_NCTF_26
- X D1 VSS_NCTF_27
- X D2 VSS_NCTF_28
- X D53 VSS_NCTF_29
- X E1 VSS_NCTF_30
- X E53 VSS_NCTF_31

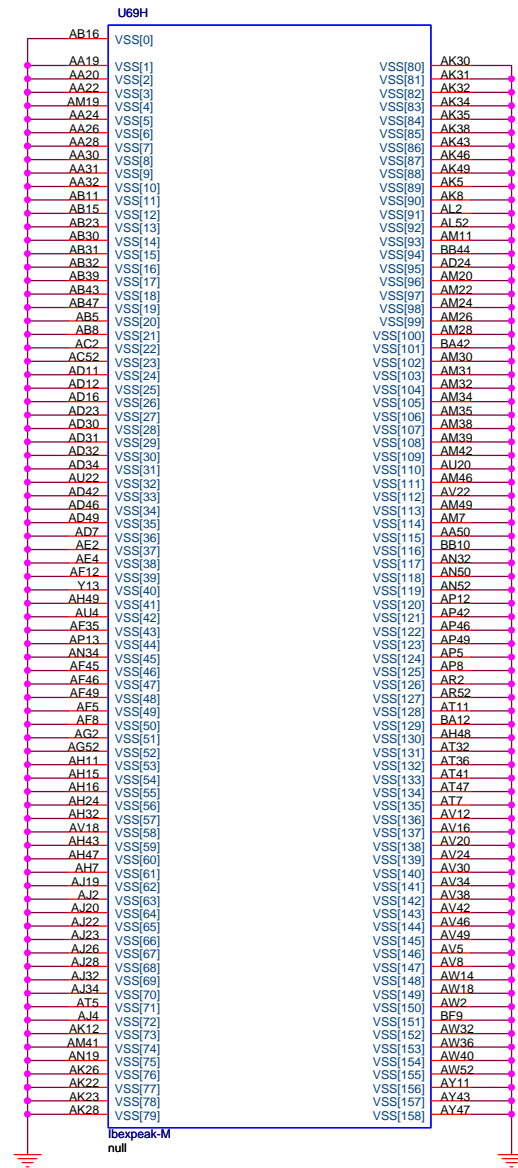
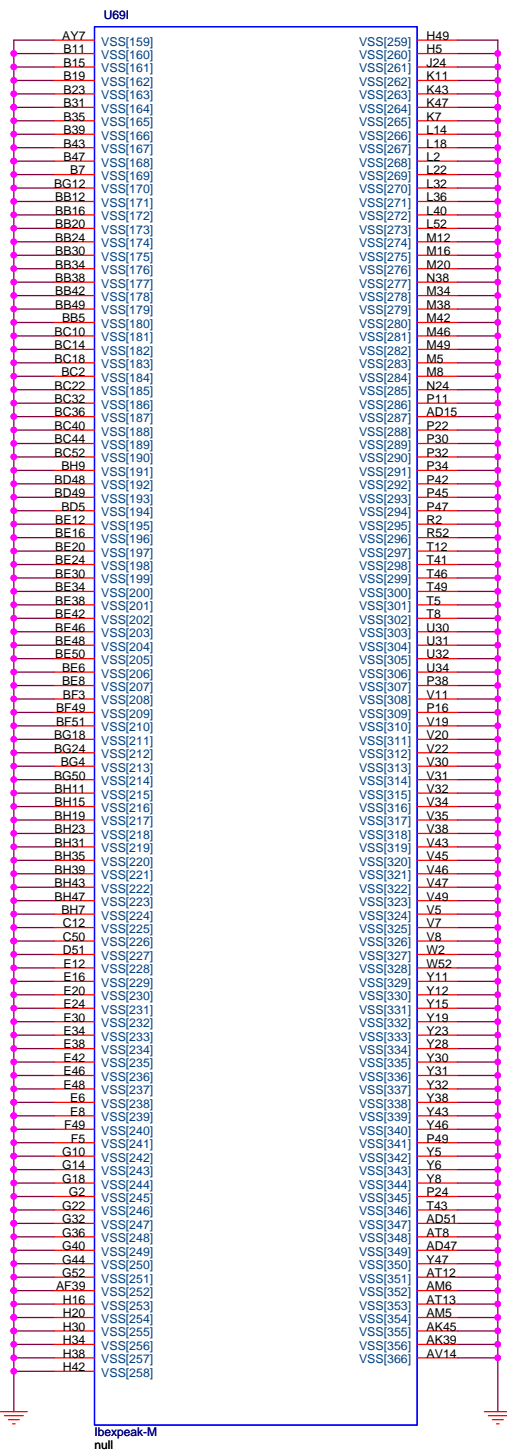


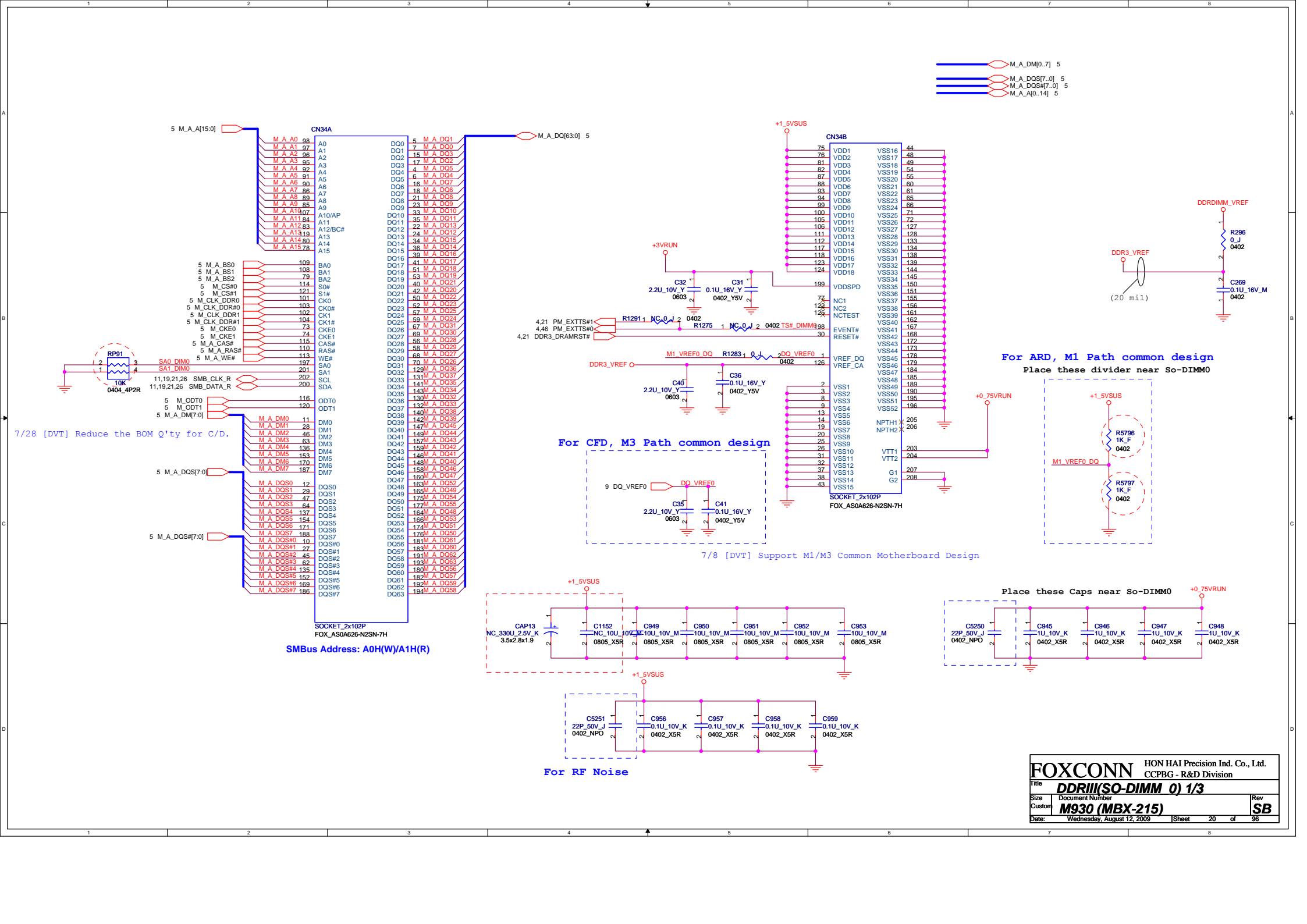
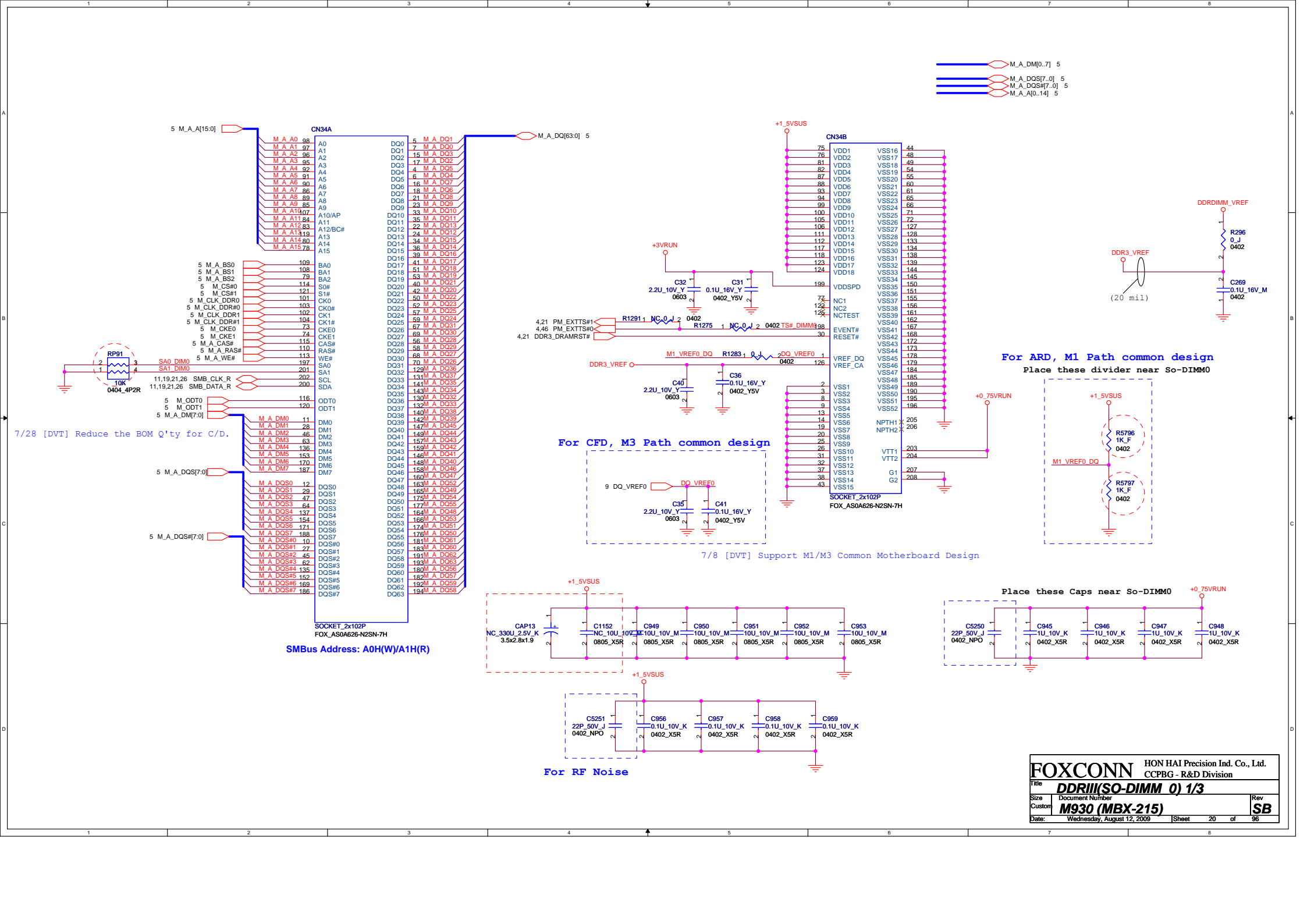
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



7/8 [DVT] Delete iGPU, Delete Dummy Parts.







7/28 [DVT] Reduce the BOM Q'ty for C/D.

For ARD, M1 Path common design
Place these divider near So-DIMM0

For CFD, M3 Path common design

7/8 [DVT] Support M1/M3 Common Motherboard Design

Place these Caps near So-DIMM0

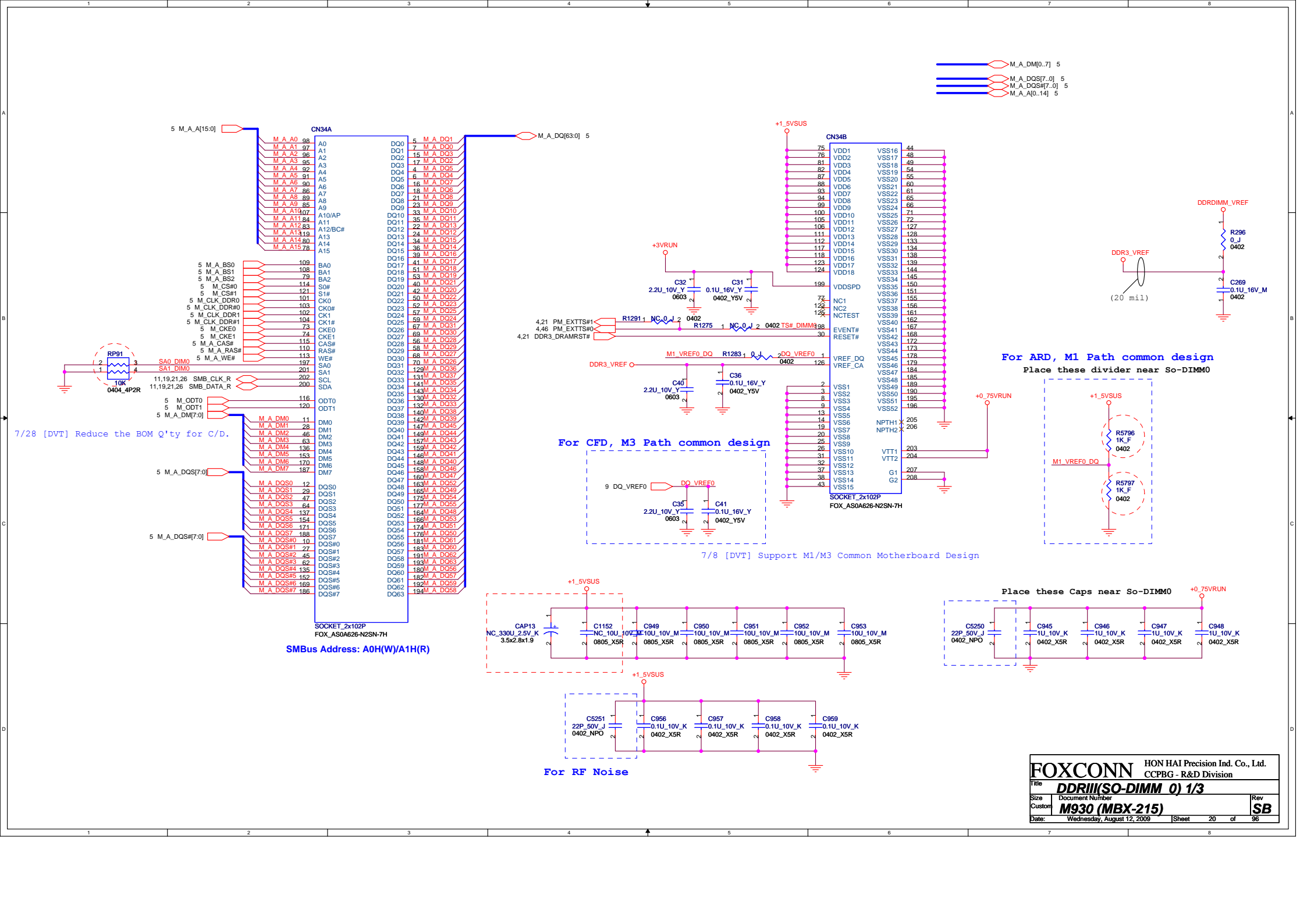
For RF Noise

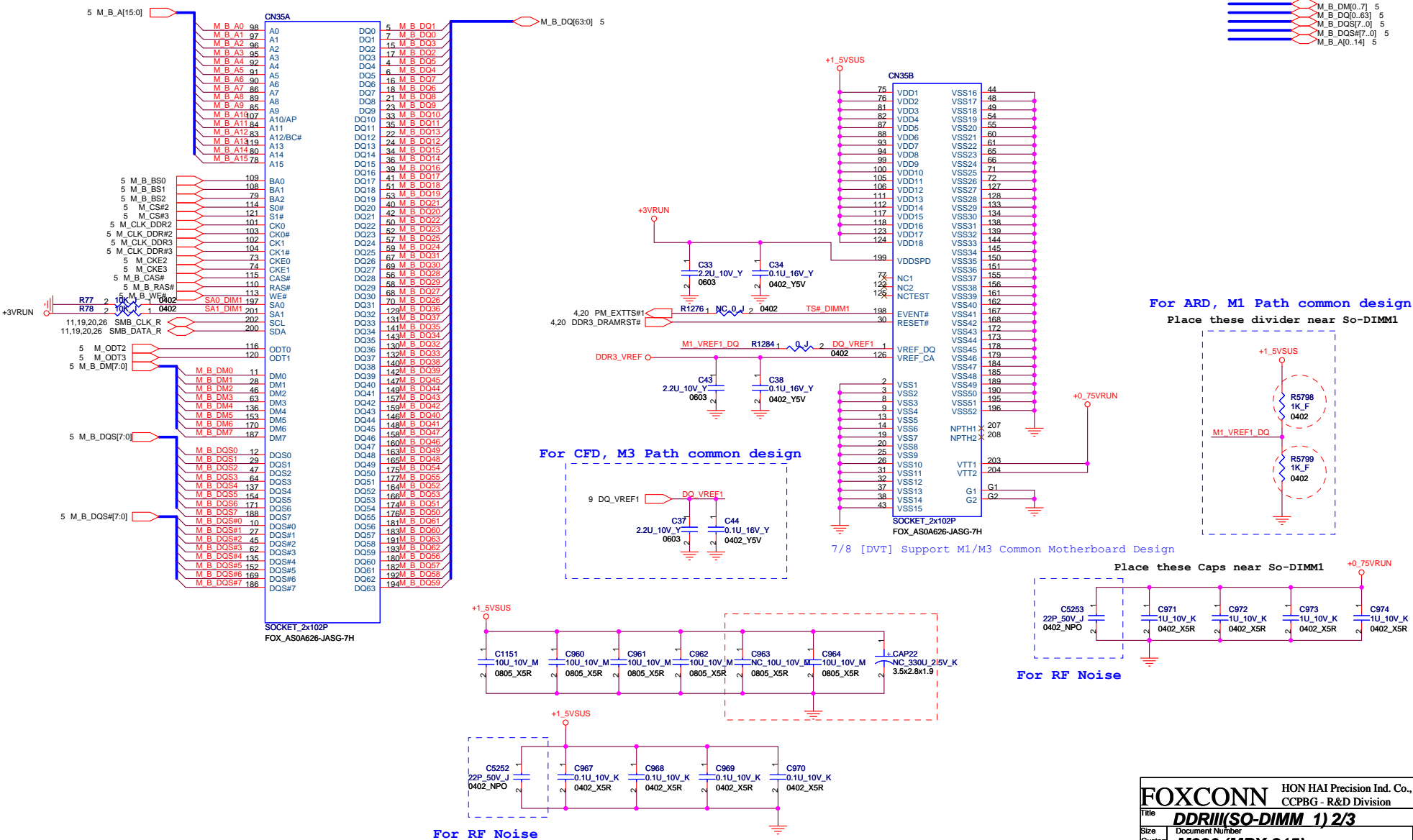
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **DDRIII(SO-DIMM 0) 1/3**

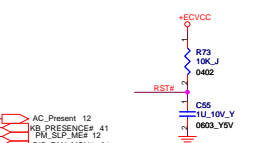
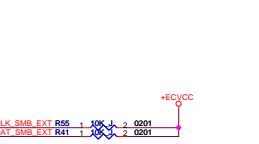
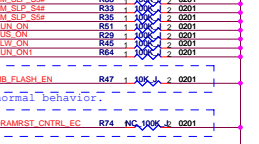
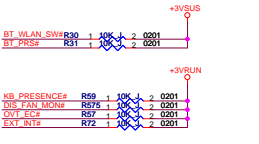
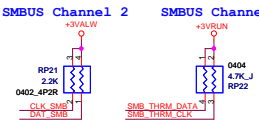
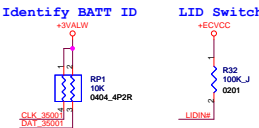
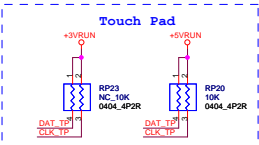
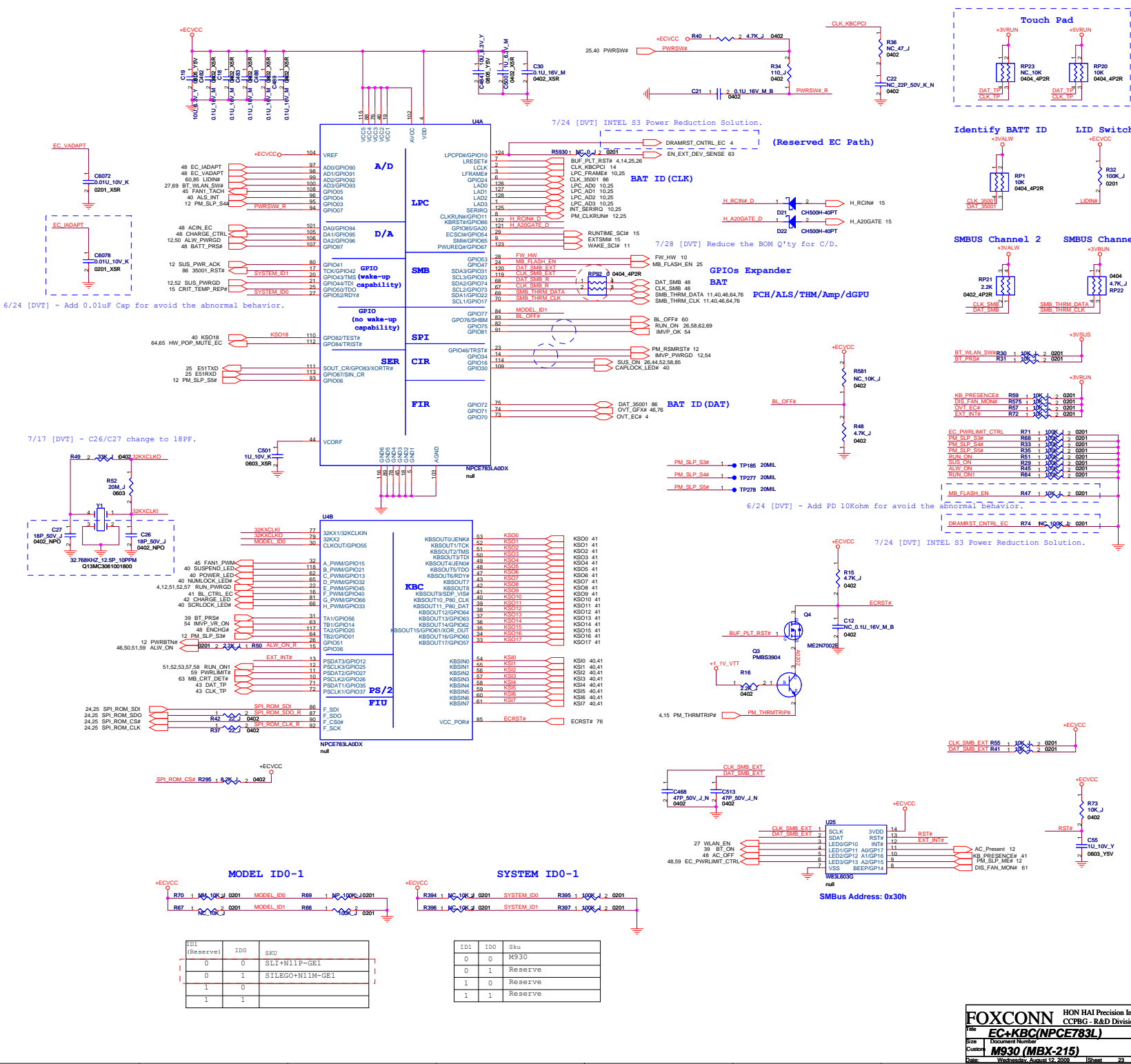
Size: Document Number
Custom: **M930 (MBX-215)**

Date: Wednesday, August 12, 2009 Sheet 20 of 96



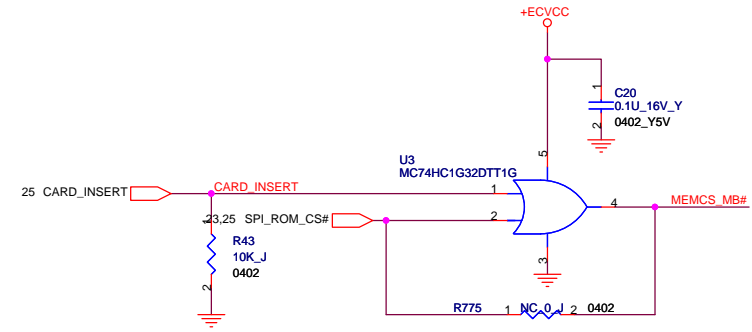
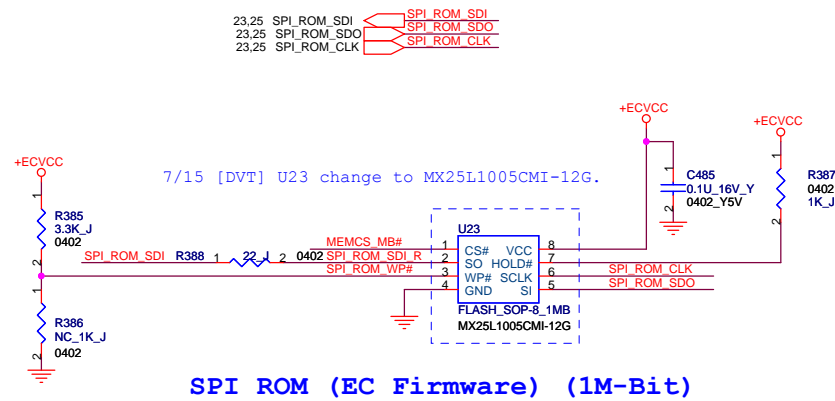


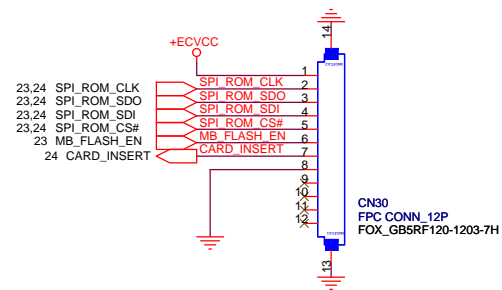
Delete M2 Path (Intel Revised)



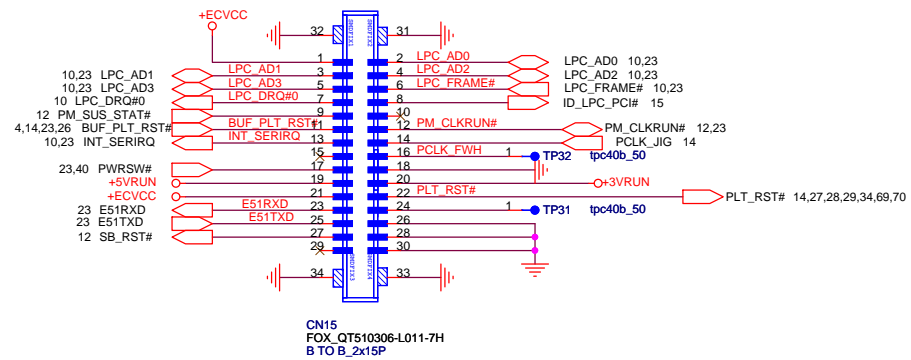
ID1 (Reserved)	ID0	SKU
0	0	SLI+N11P-GE1
0	1	SLI+GO+N11M-GE1
1	0	
1	1	

ID1	ID0	SKU
0	0	M930
0	1	Reserved
1	0	Reserved
1	1	Reserved

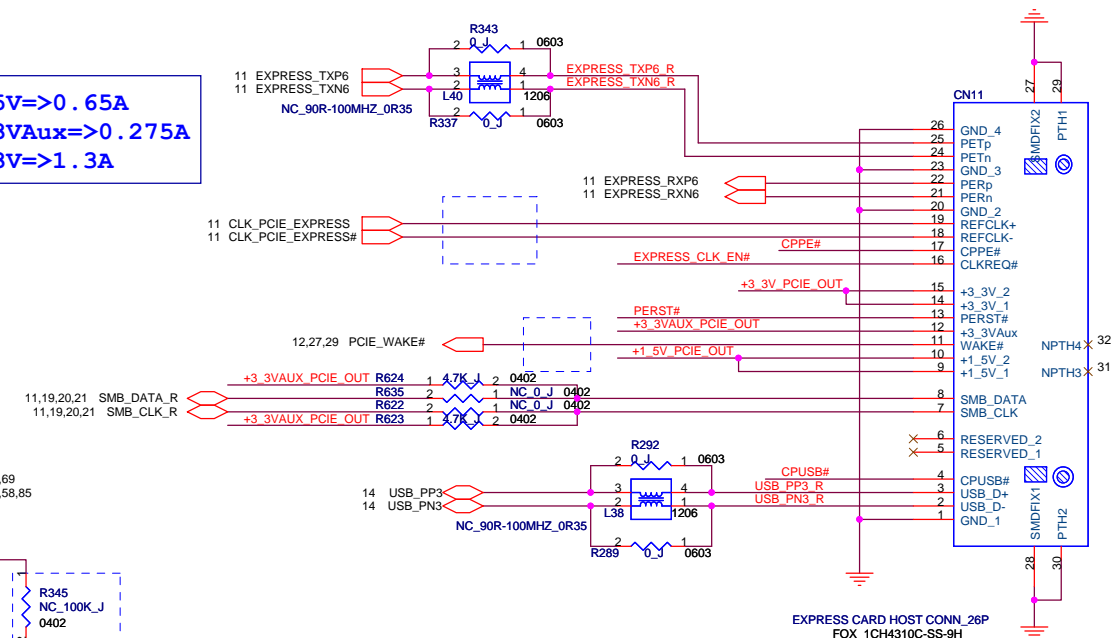
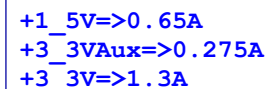
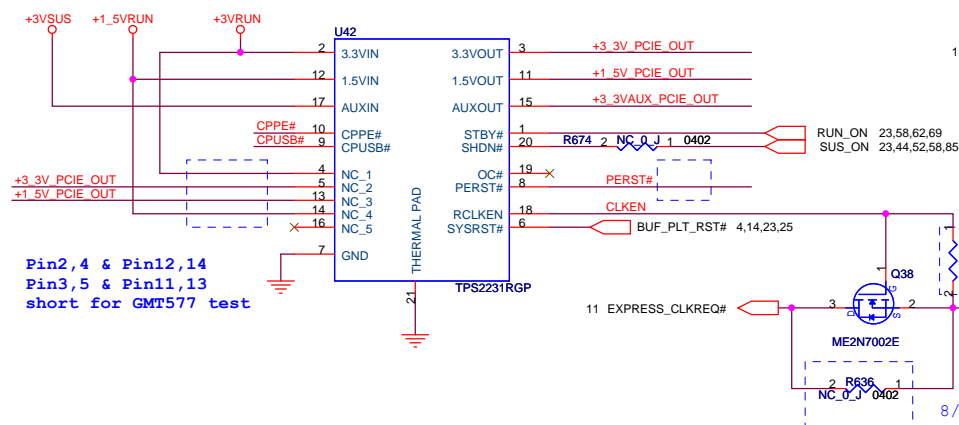




EXTERNAL SPI ROM INTERFACE (EC)

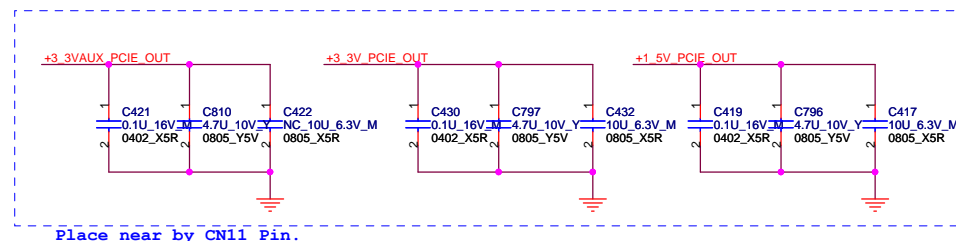
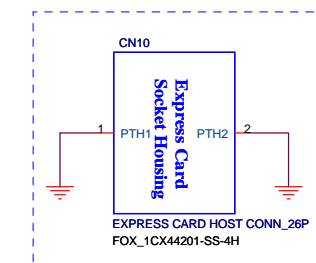
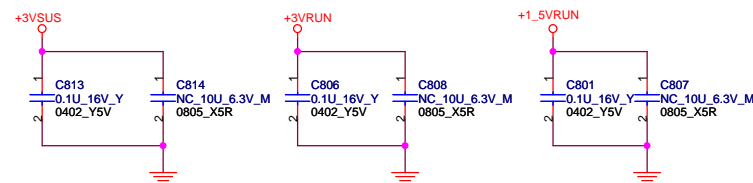


JIG-120

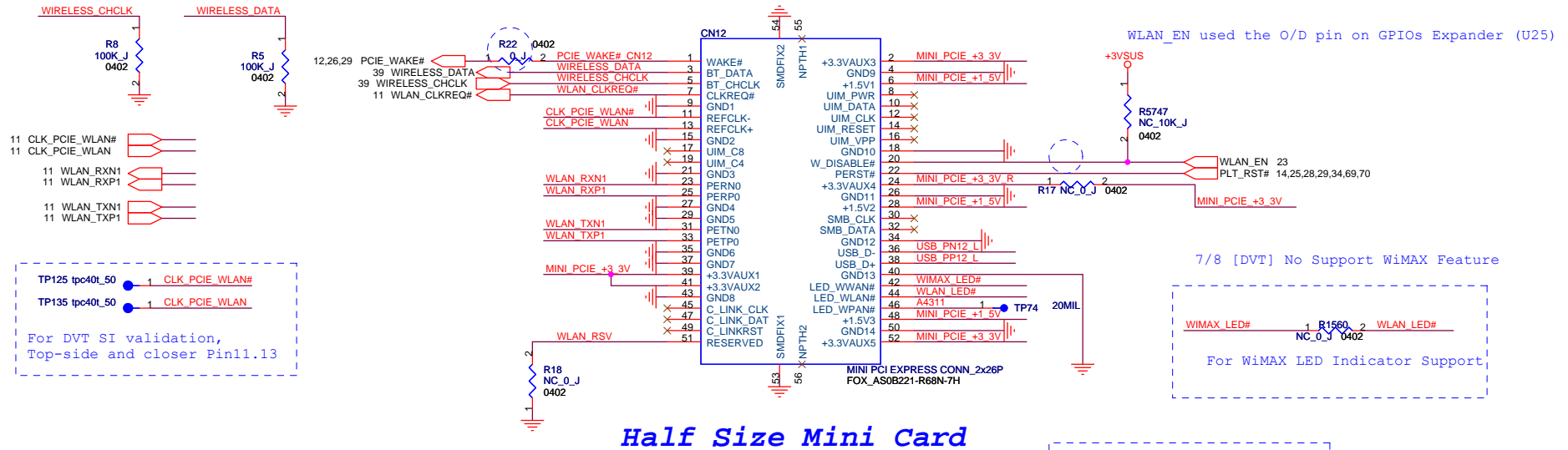


7/23 [DVT] Add R345 for MOR request. (Reserve)

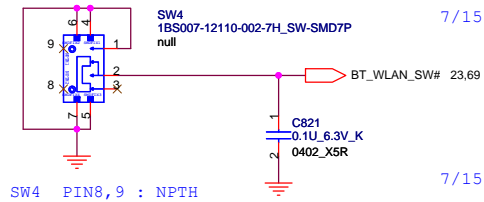
8/10 [DVT] Add R636 for MOR request. (Reserve)



8/3 [DVT] Reserve R22 as MOR request. (WoWLAN Function)



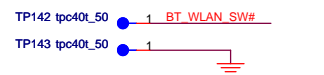
WLAN Switch



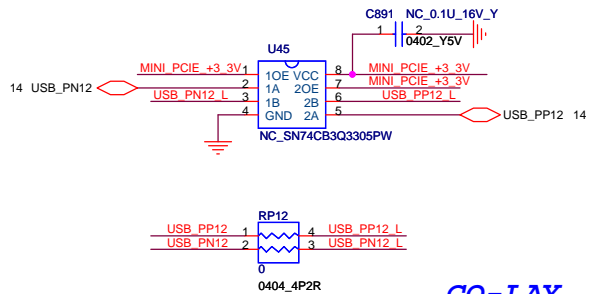
7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)



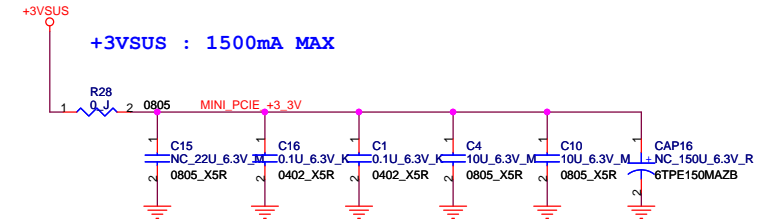
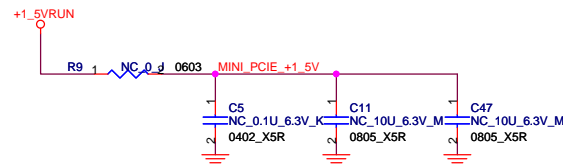
7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)

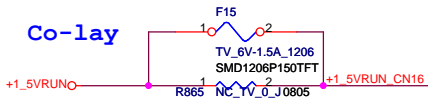
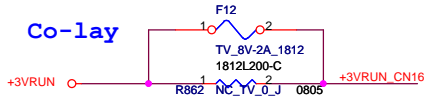


USB I/F for Wi-MAX(Kilmer Peak)



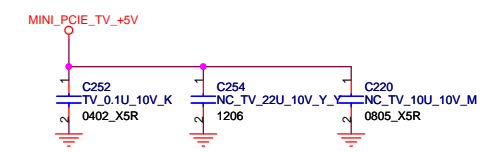
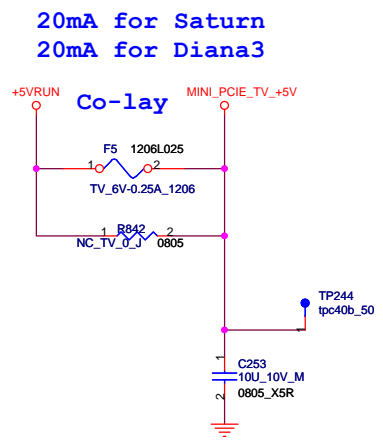
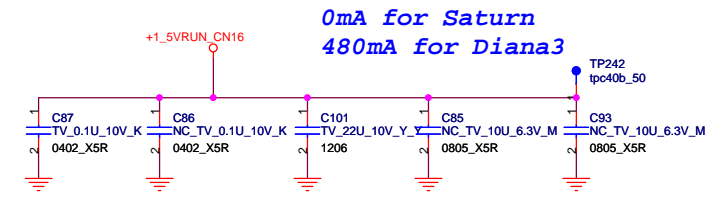
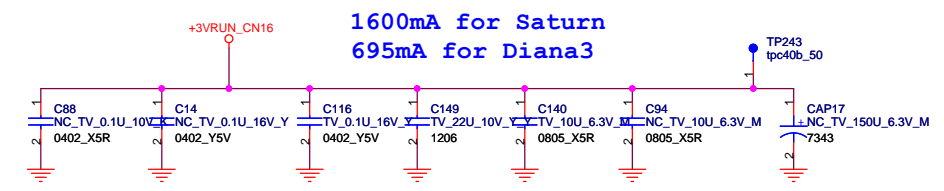
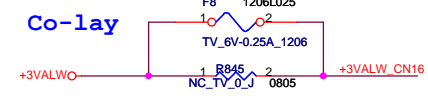
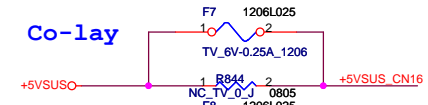
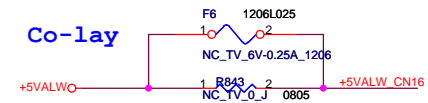
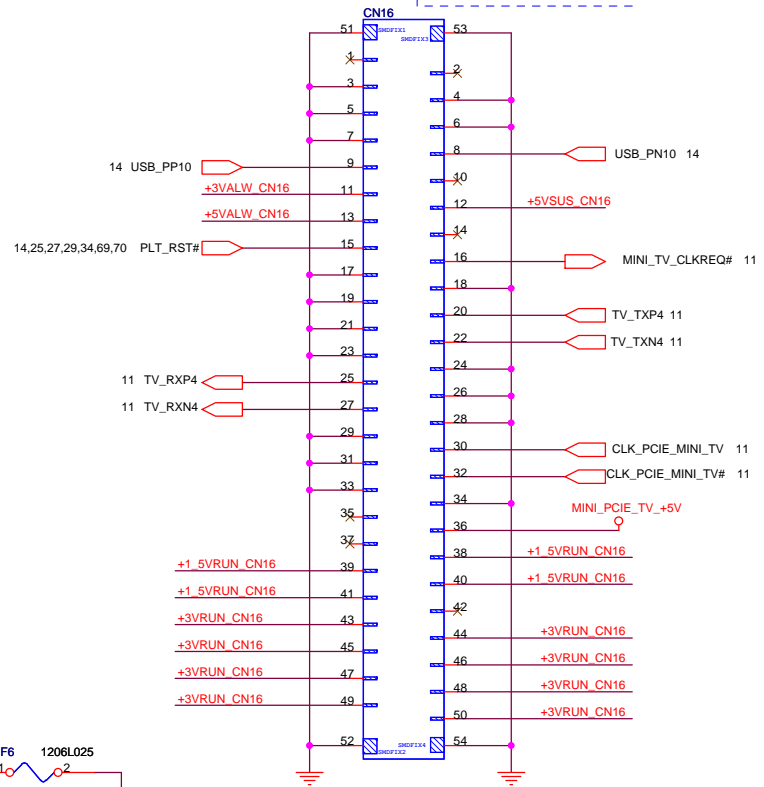
+1_5VRUN : 330mA MAX
Intel Puma Peak & Kilmer Peak nonsupport +1_5VRUN





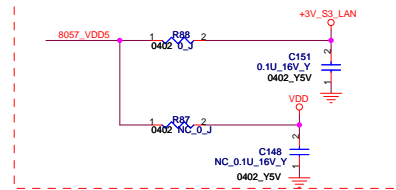
7/13 [DVT] CN16 change to GB12501-10510-7H

TV_FPC CONN_50P
FOX_GB12501-10510-7H

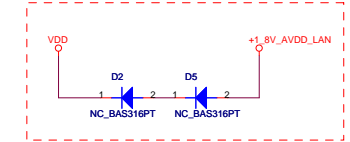
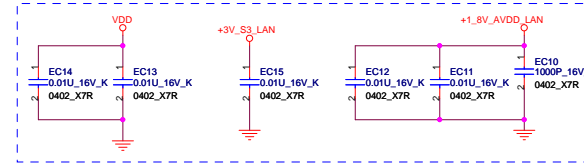




For 8059 Dummy R88, C151, and Stuff R87, C148
For 8057 Dummy R87, C148 and Stuff R88, C151

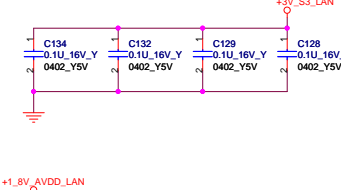
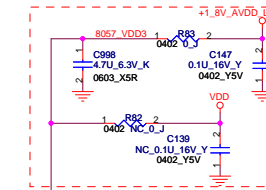
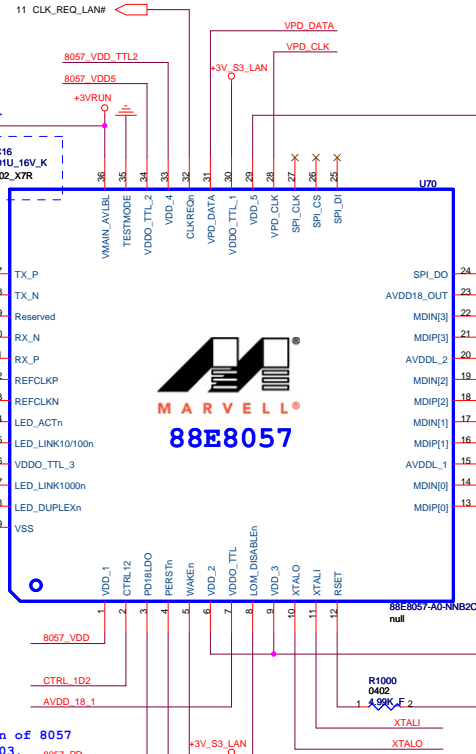


8/5 [DVT]Add EC10-EC15 for EMI Solution.

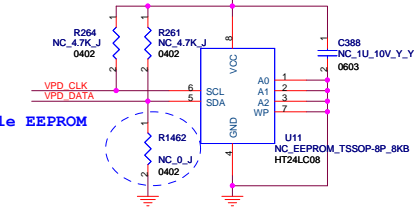


8/5 [DVT]Add EC16 for EMI Solution.

For 8059 Stuff R97
For 8057 Dummy R97

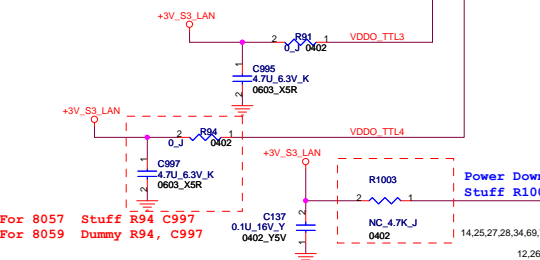


For Disable EEPROM

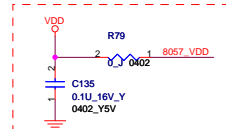


Place C993/C994
close as U70 pin

For 8059 Stuff R89, R90, C993, C994
For 8057 Dummy R89, R90, C993, C994

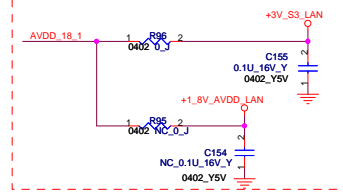


For 8059 Z0 version ONLY, Dummy R1003
For 8059 A0 version ONLY, Stuff R1003

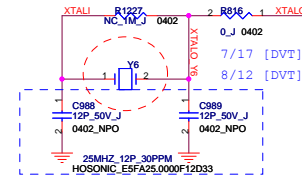


Dummy all when use 88E8059 (A0/Z0)

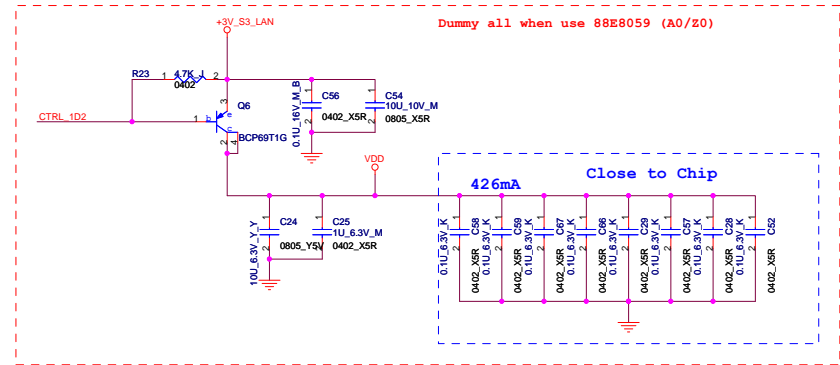
For 8059 Dummy R96, C155, and Stuff R85, C154
For 8057 Dummy R95, C154 and Stuff R96, C155

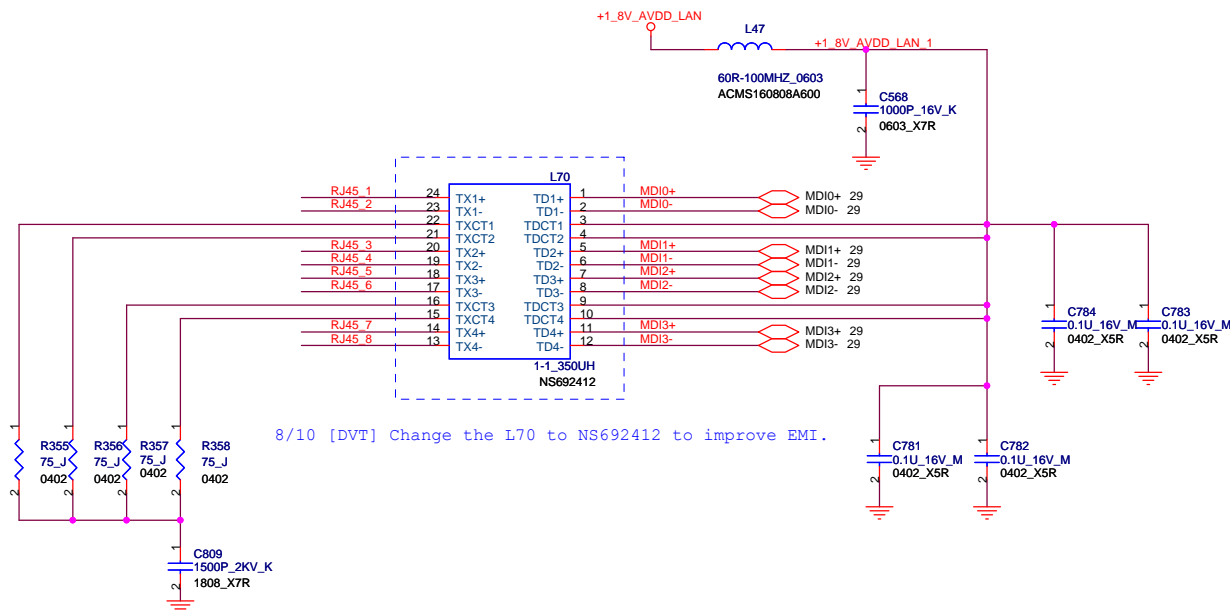


7/8 [DVT] Change the C988, C989 CL value to 12P.

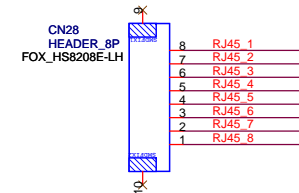


Dummy all when use 88E8059 (A0/Z0)

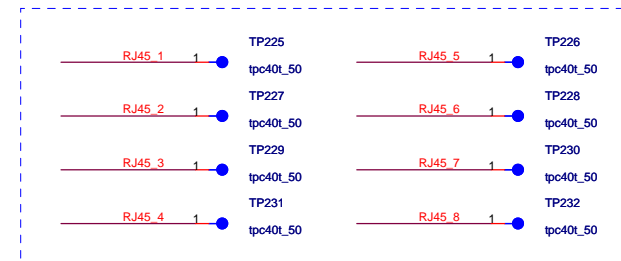




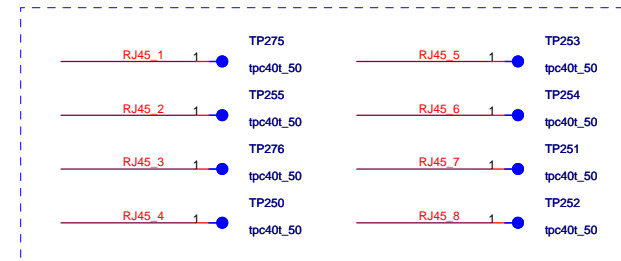
8/10 [DVT] Change the L70 to NS692412 to improve EMI.



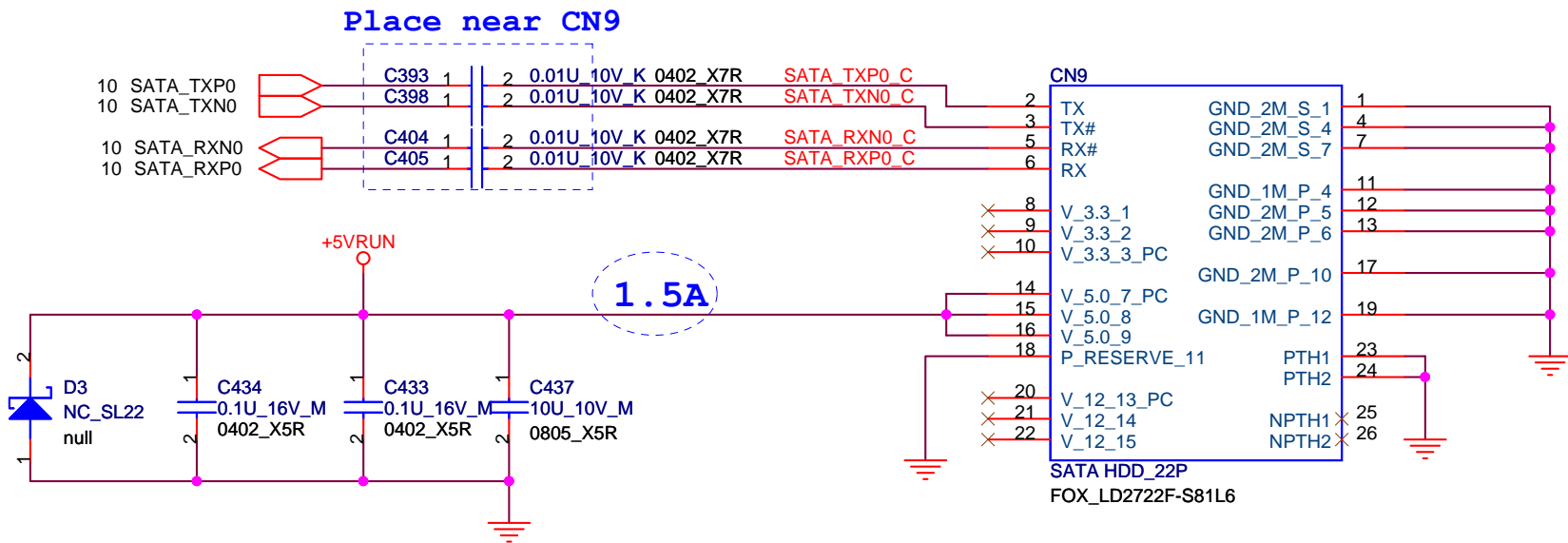
RJ45



7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)

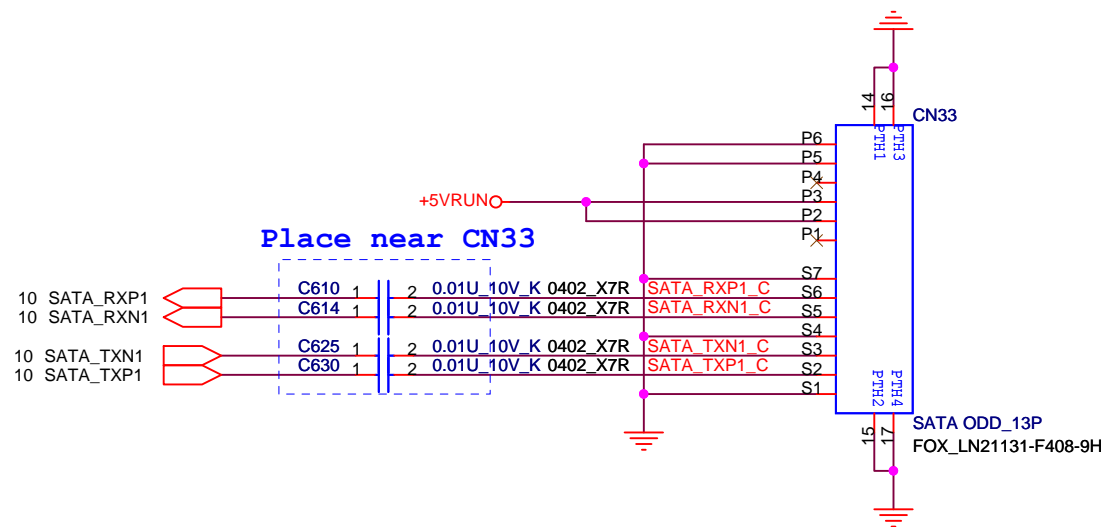


7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)

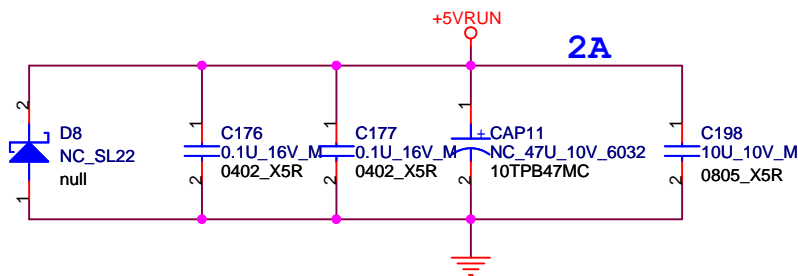


SATA HDD CONN

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title SATA HDD			
Size A	Document Number M930 (MBX-215)		Rev SB
Date:	Wednesday, August 12, 2009	Sheet 31 of 96	



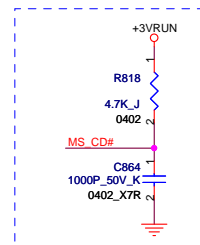
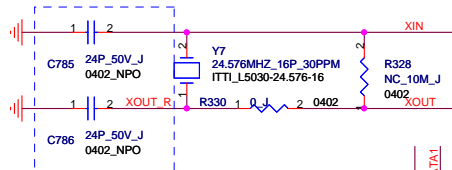
SATA ODD CONN



Remove Braidwood (Intel Updated and MOR confirmed)

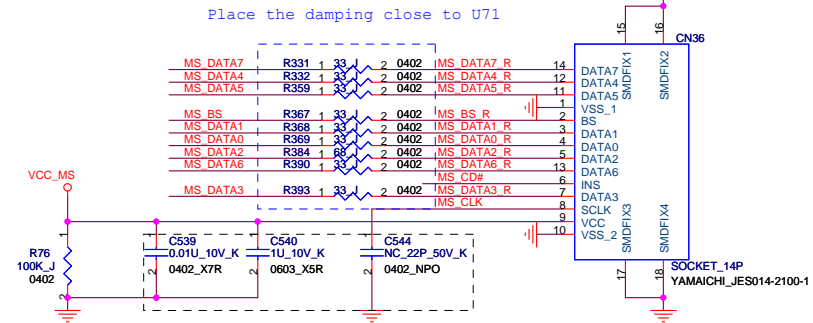
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Braidwood Connector			
Size	Document Number		Rev
Custom	M930 (MBX-215)		SB
Date:	Wednesday, August 12, 2009		Sheet 33 of 96

7/9 [DVT] Change C785/C786 value to 24P depends on Cystal report.



Place the R/C close to U71

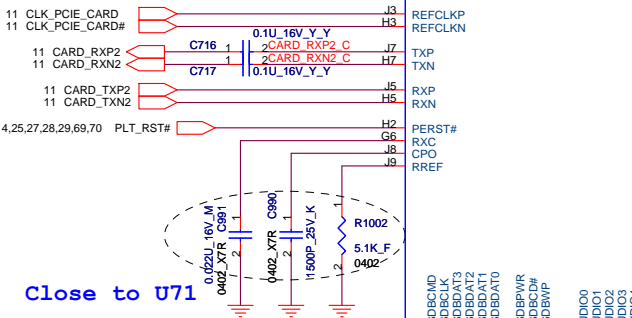
7/8 [DVT] Change Damping value to fix the OS/US issue.



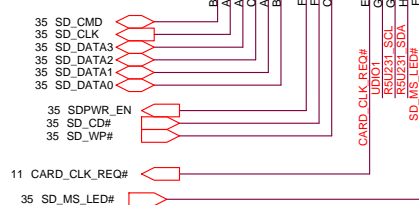
Place the damping close to U71

Place the CAP close to CN36

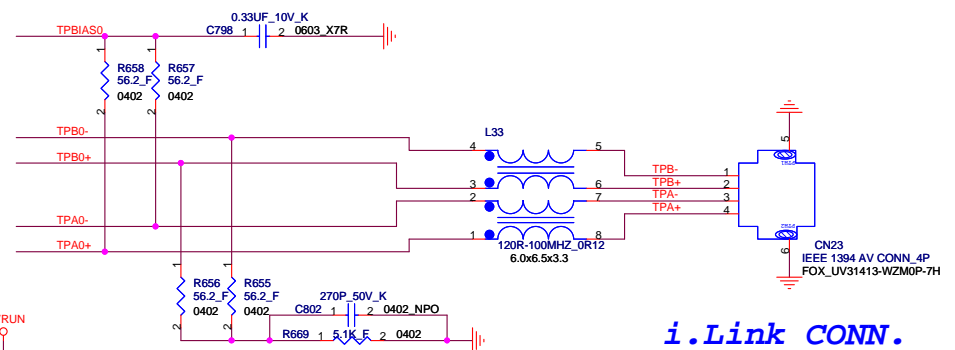
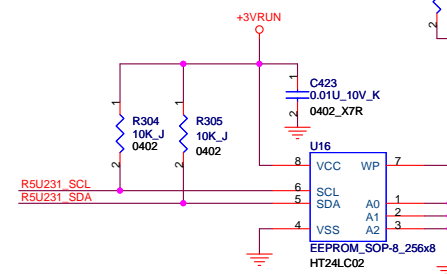
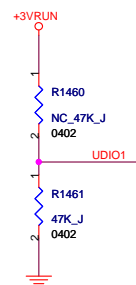
MS HG-DUO CONN.



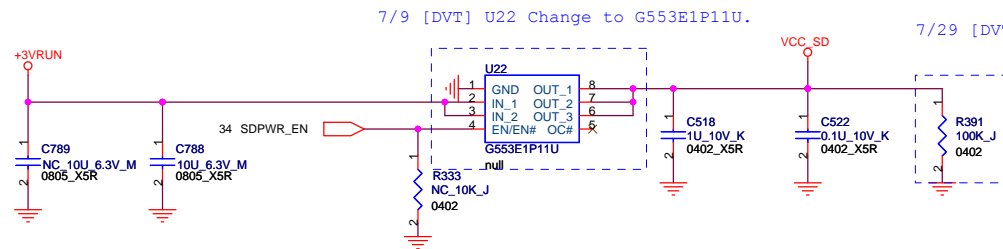
Close to U71



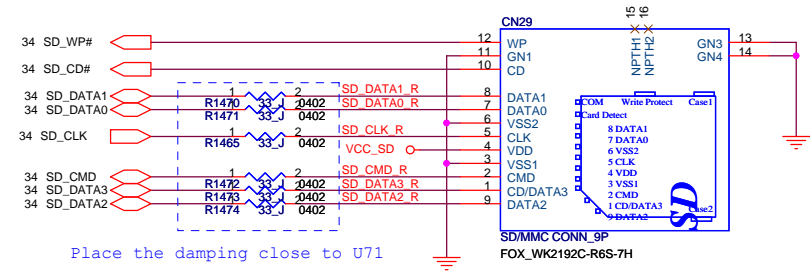
SR0M: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)



i.Link CONN.

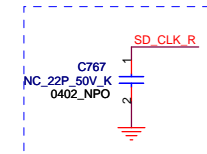
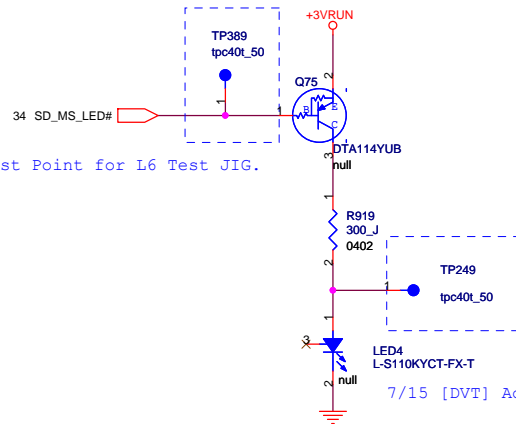


SD POWER

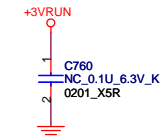


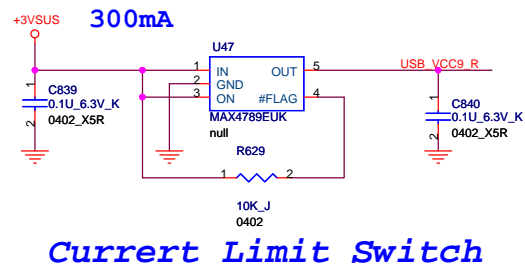
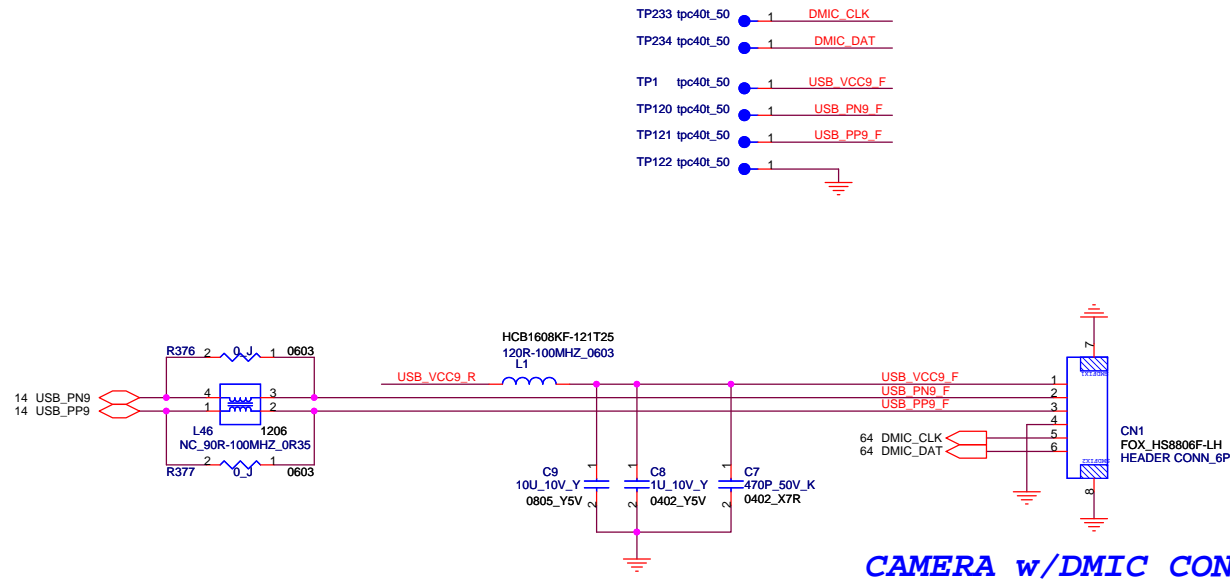
7/8 [DVT] Change Damping value to fix the OS/US issue.

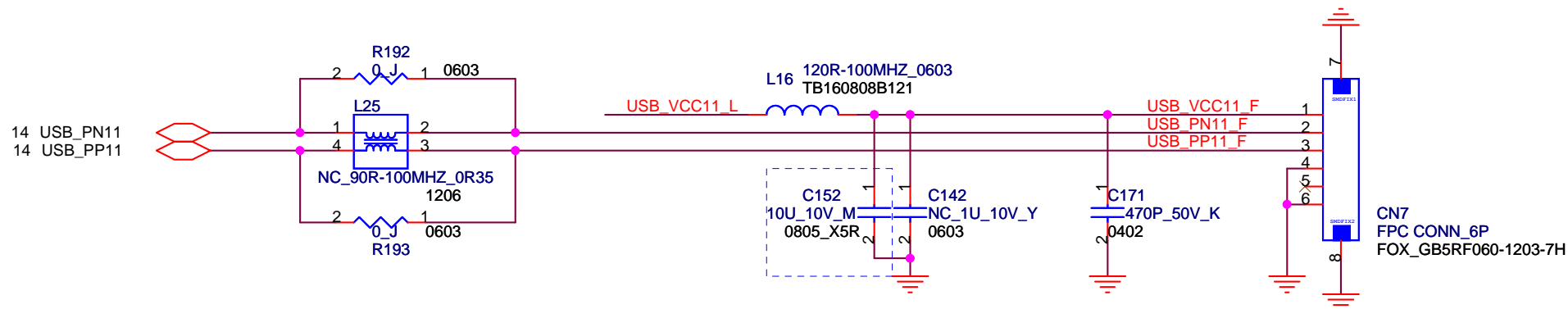
SD CONN.



8/5 [DVT] Dummy C767 and Change R1465 to 33ohm.

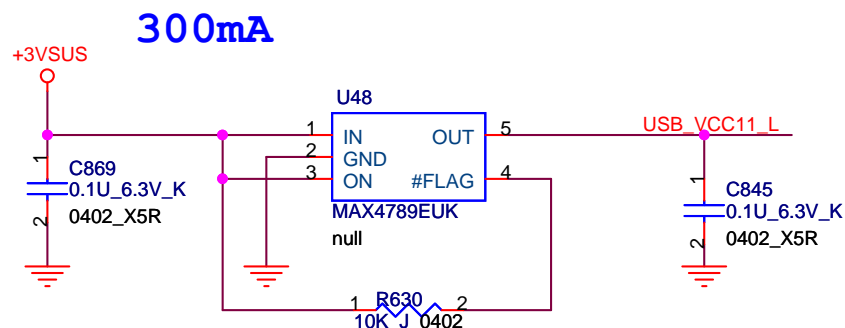




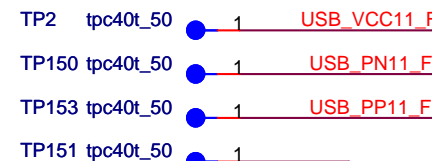


Felica Conn.

Felica Vdd Spec. (3.15V to 3.45V)



Current Limit Switch



7/15 [DVT] Add Test Point for L6 JIG.(Top-side)

FOXCONN

HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

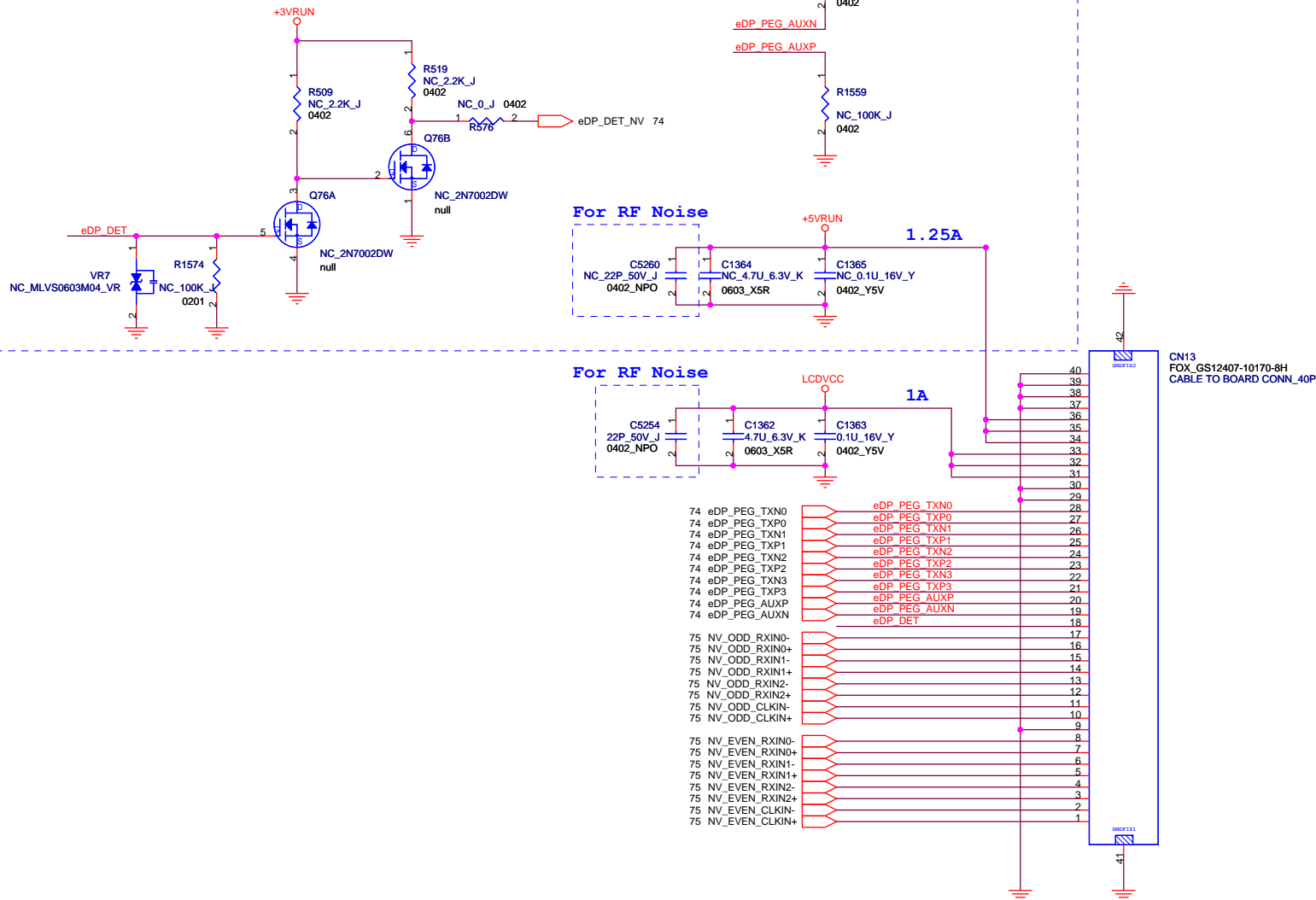
Title **Felica Connector**

Size A Document Number **M930 (MBX-215)**

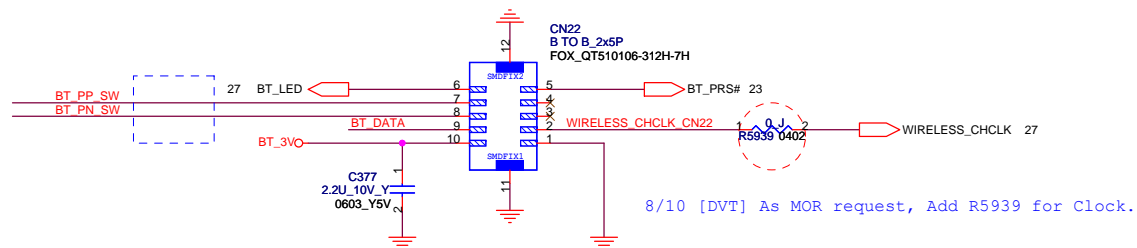
Rev **SB**

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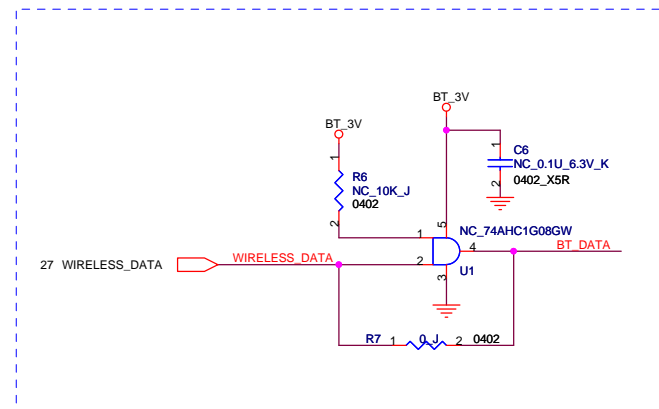
eDP (Suzaku3 support) >> Stuff



eDP & LVDS CONNECTOR

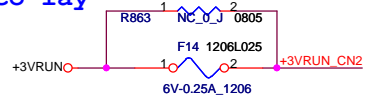


Bluetooth CONN.



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <i>Bluetooth Connector</i>			
Size	Document Number	Rev	
Custom	<i>M930 (MBX-215)</i>	<i>SB</i>	
Date:	Wednesday, August 12, 2009	Sheet	39 of 96

Co-lay



Light Sensor (EC)

11,23,46,64,76 SMB_THRM_DATA
11,23,46,64,76 SMB_THRM_CLK
23 ALS_INT

Switch Keyboard Matrix

Keyboard LED

Power Button

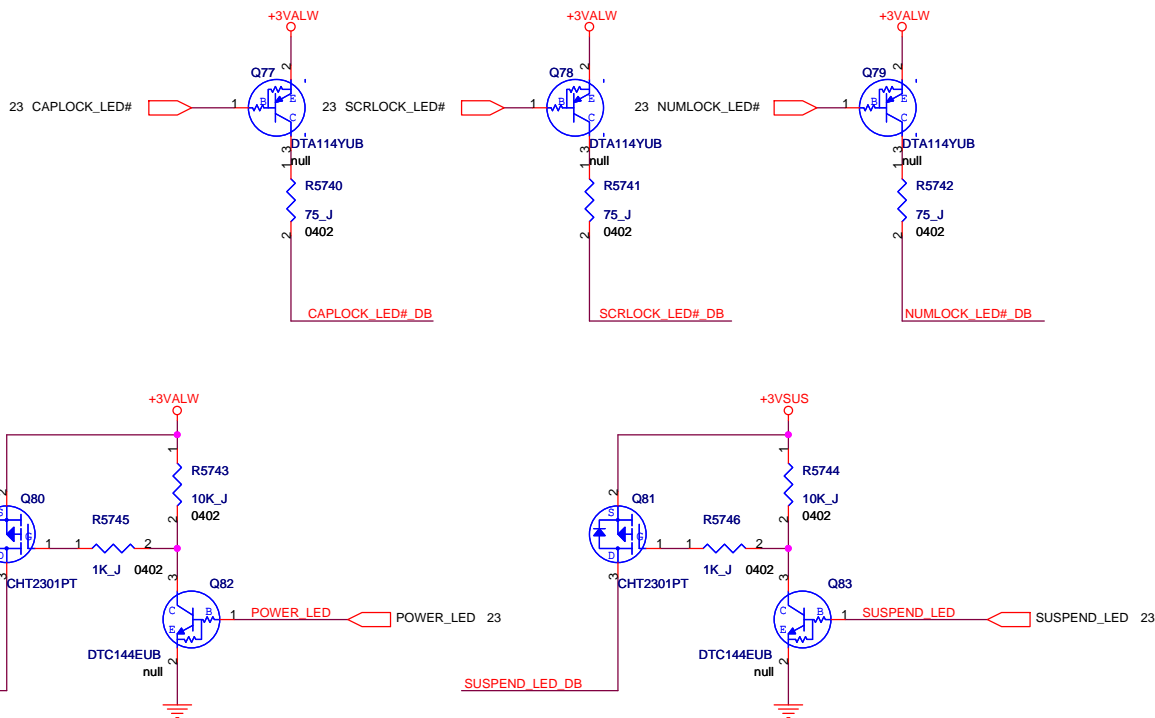
23 KSO18
23,41 KSI0
23,41 KSI1
23,41 KSI2
23,41 KSI3
23,41 KSI4
23,41 KSI5
23,41 KSI6
23,41 KSI7

NUMLOCK_LED#_DB
SCRLOCK_LED#_DB
CAPLOCK_LED#_DB
POWER_LED_DB
SUSPEND_LED_DB

23,25 PWRSW#

CN2
FPC CONN_24P
FOX_GB5RF240-1203-7H

Switch DB Conn.



TP385 tpc40b_50 1 PWRSW#
TP376 tpc40b_50 1

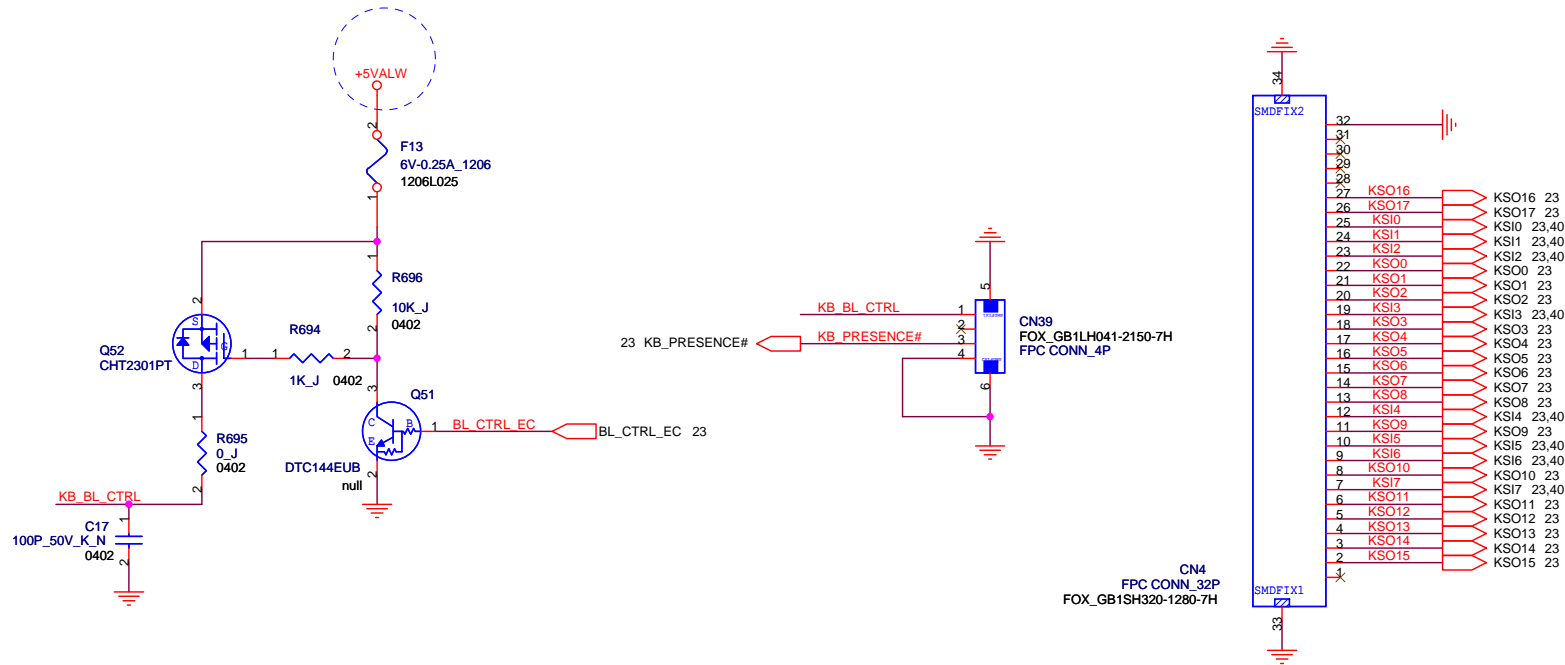
Top side ,Closer together

TP462 tpc40b_50 1 PWRSW#
TP384 tpc40b_50 1

Bot side ,Closer together

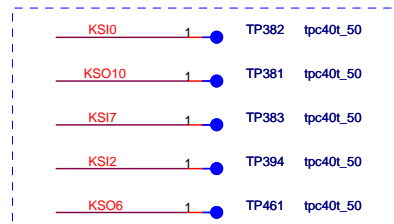
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Switch DB Connector		
Size	Document Number		Rev
Custom	M930 (MBX-215)		SB
Date:	Wednesday, August 12, 2009	Sheet	40 of 96

6/24 [DVT] - EC Engineer Request, for Backlit control well.

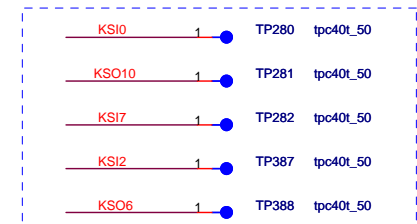


Backlit Power Conn

KBC Conn (Refer to the M780)

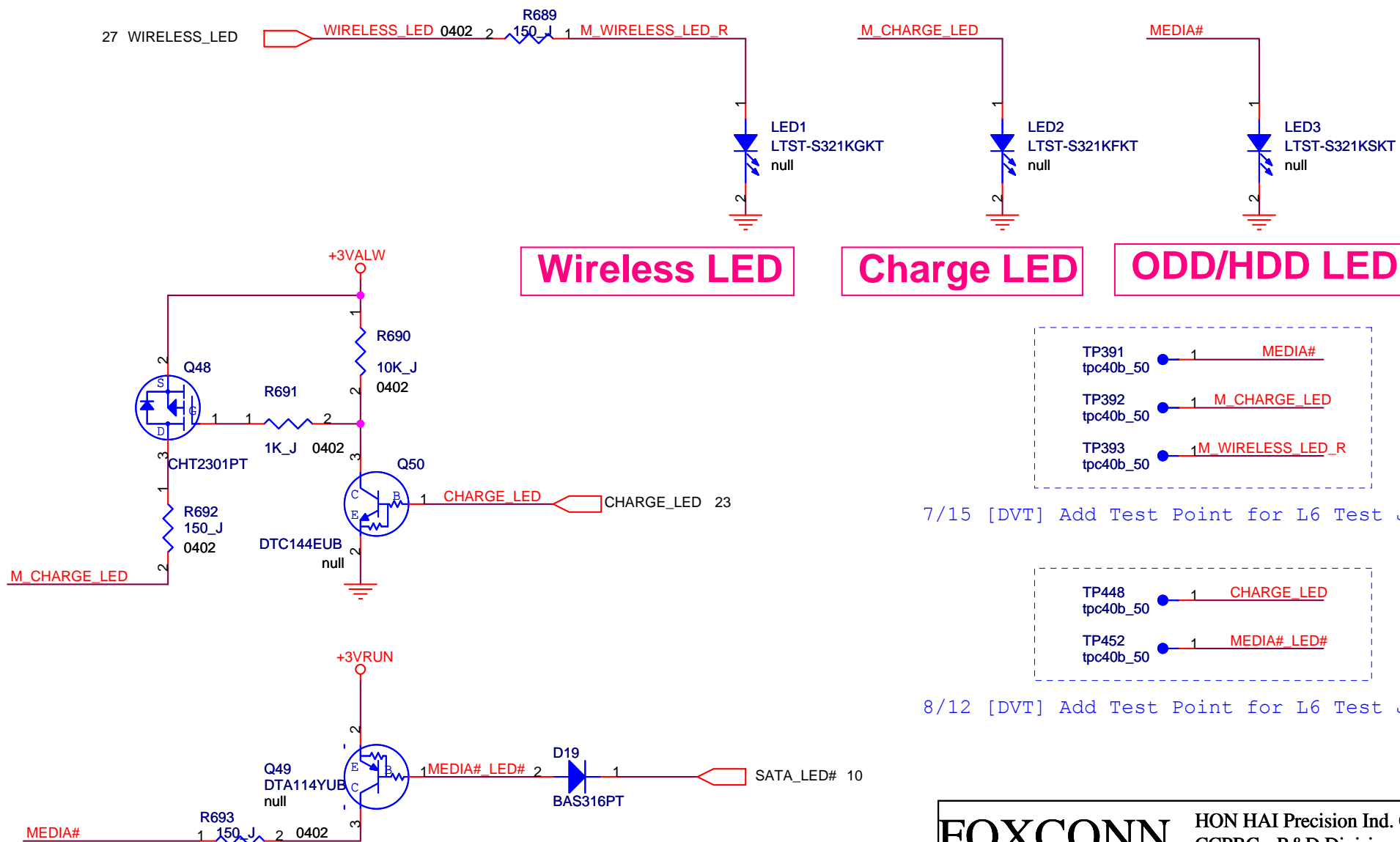


7/15 [DVT] Add Test Point for L6 Test JIG. (Bot-side)



7/15 [DVT] Add Test Point for L6 Test JIG. (Top-side)

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title KB & Backlit Connector			
Size	Document Number		Rev
B	M930 (MBX-215)		SB
Date:	Wednesday, August 12, 2009		Sheet 41 of 96



7/15 [DVT] Add Test Point for L6 Test JIG.

8/12 [DVT] Add Test Point for L6 Test JIG.

FOXCONN

HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

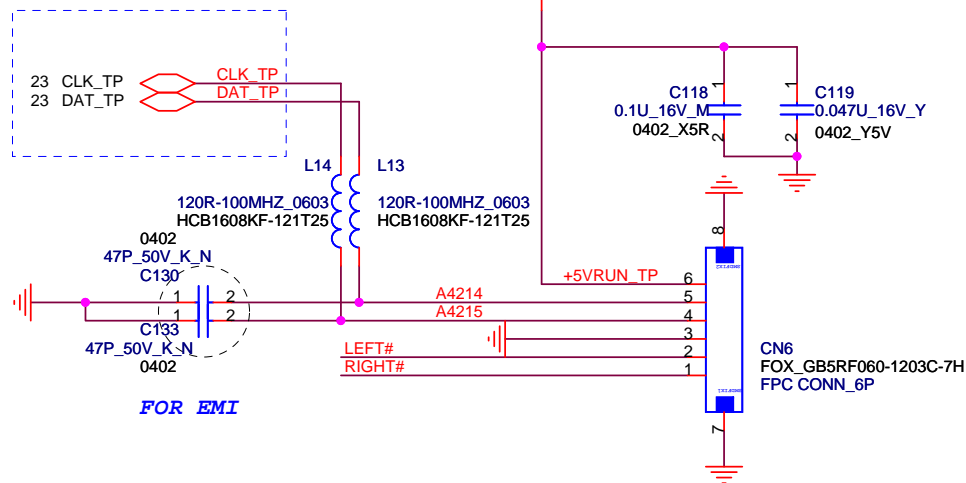
Title **Status LED**

Size A Document Number **M930 (MBX-215)**

Rev **SB**

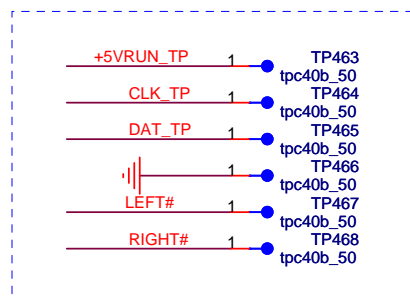
Date: Wednesday, August 12, 2009 Sheet 42 of 96

+5VRUN > R533 ,RP20 Stuff
+3VRUN > R530, RP23 Stuff



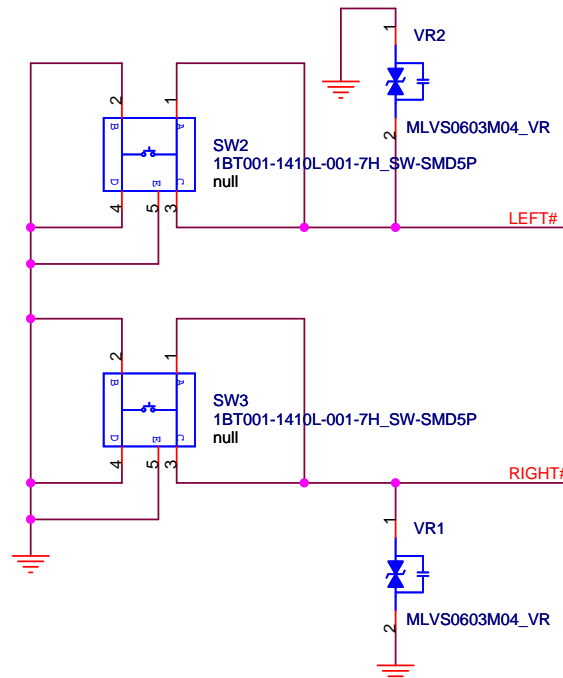
FOR ALPS TOUCH PAD

Touch Pad Conn (Support Multi Touch)



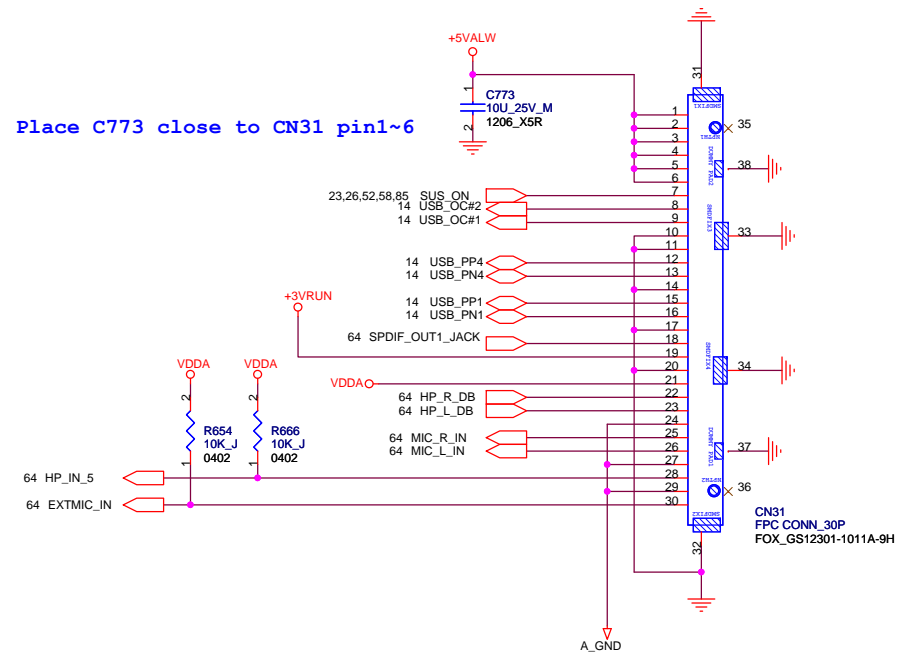
7/15 [DVT] Add Test Point for L6 JIG.(Bot-side)

TP_LEFT Button

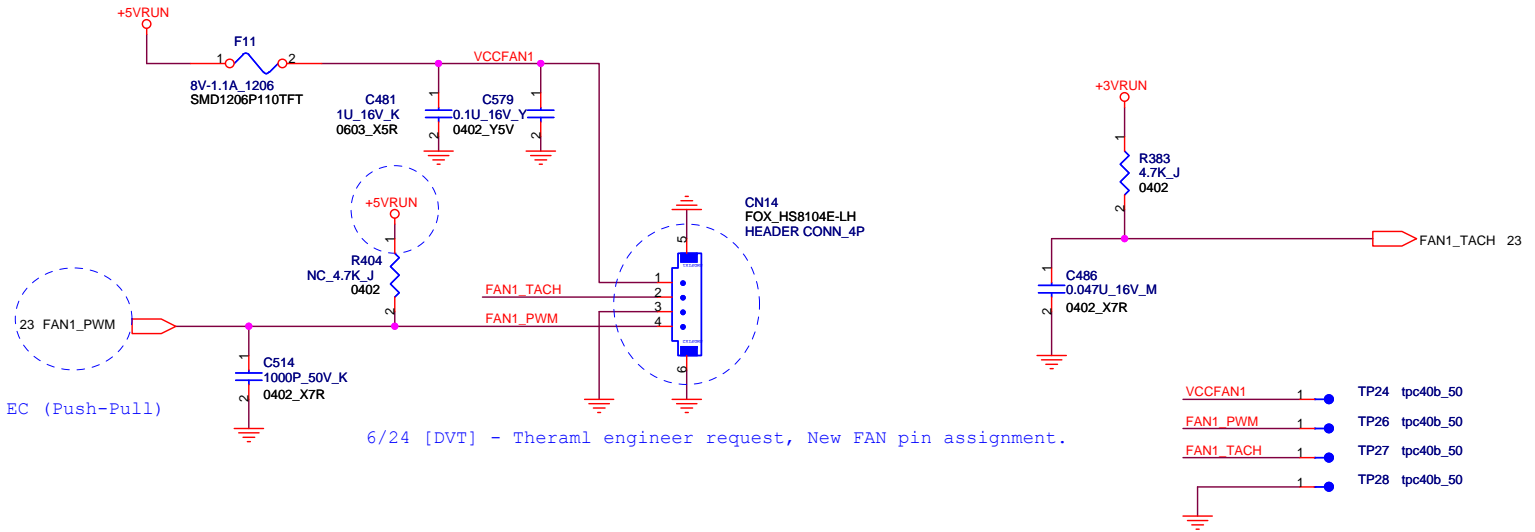


TP_Right Button

FOXCONN		HON HAI Precision Ind. Co., Ltd.
		CCPBG - R&D Division
Title	Touch Pad	
Size	Document Number	Rev
Custom	M930 (MBX-215)	SB
Date:	Wednesday, August 12, 2009	Sheet 43 of 96



Direct PWM FAN



[illegible]

Adaptor
19.5V / 120W

TI
BQ24753A
Battery Charger
Switch Mode
PAGE 48

Battery
Li-ion
11.1V
5200mAh
4800mAh
4400mAh

TI
SN0608098
Switch Mode
FOR System
PAGE 50

TI / GMT
TPS51218 + G2998
Switch Mode
FOR DDR3
PAGE 52

TI
TPS51218
Switch Mode
FOR VTT=>+1.1V VTT
PAGE 51

TI
TPS51218
Switch Mode
FOR PCH
PAGE 51

MAXIM
MAX17030
Switch Mode
FOR CPU Core
PAGE 54

MAXIM
MAX17028
Switch Mode
FOR +VCC_GFXCORE
PAGE 56

TI
TPS51217
Switch Mode
FOR D_VGA
PAGE 57

System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
+3VSUS/1.5A
N-Channel transistor
+3VRUN/5A
N-Channel transistor
+1_8VRUN/2A
APL5912 LDO
+1_5VRUN/4A
N-Channel transistor
+1_5VSUS/14A
N-Channel transistor
+0_75VRUN/2A
APL9513 LDO
PEX_VDD/2.5A
+5VALW_LDO
AT5208 LDO
+ECVCC/100mA
+12V For Load switch
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
+3VSUS/1.5A
N-Channel transistor
+3VRUN/5A
N-Channel transistor
+1_8VRUN/2A
APL5912 LDO
+1_5VRUN/4A
N-Channel transistor
+1_5VSUS/14A
N-Channel transistor
+0_75VRUN/2A
APL9513 LDO
PEX_VDD/2.5A
+5VALW_LDO
AT5208 LDO
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+12V For Load switch
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
+3VSUS/1.5A
N-Channel transistor
+3VRUN/5A
N-Channel transistor
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N-Channel transistor
+0_75VRUN/2A
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+5VALW_LDO
AT5208 LDO
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+12V For Load switch
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+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

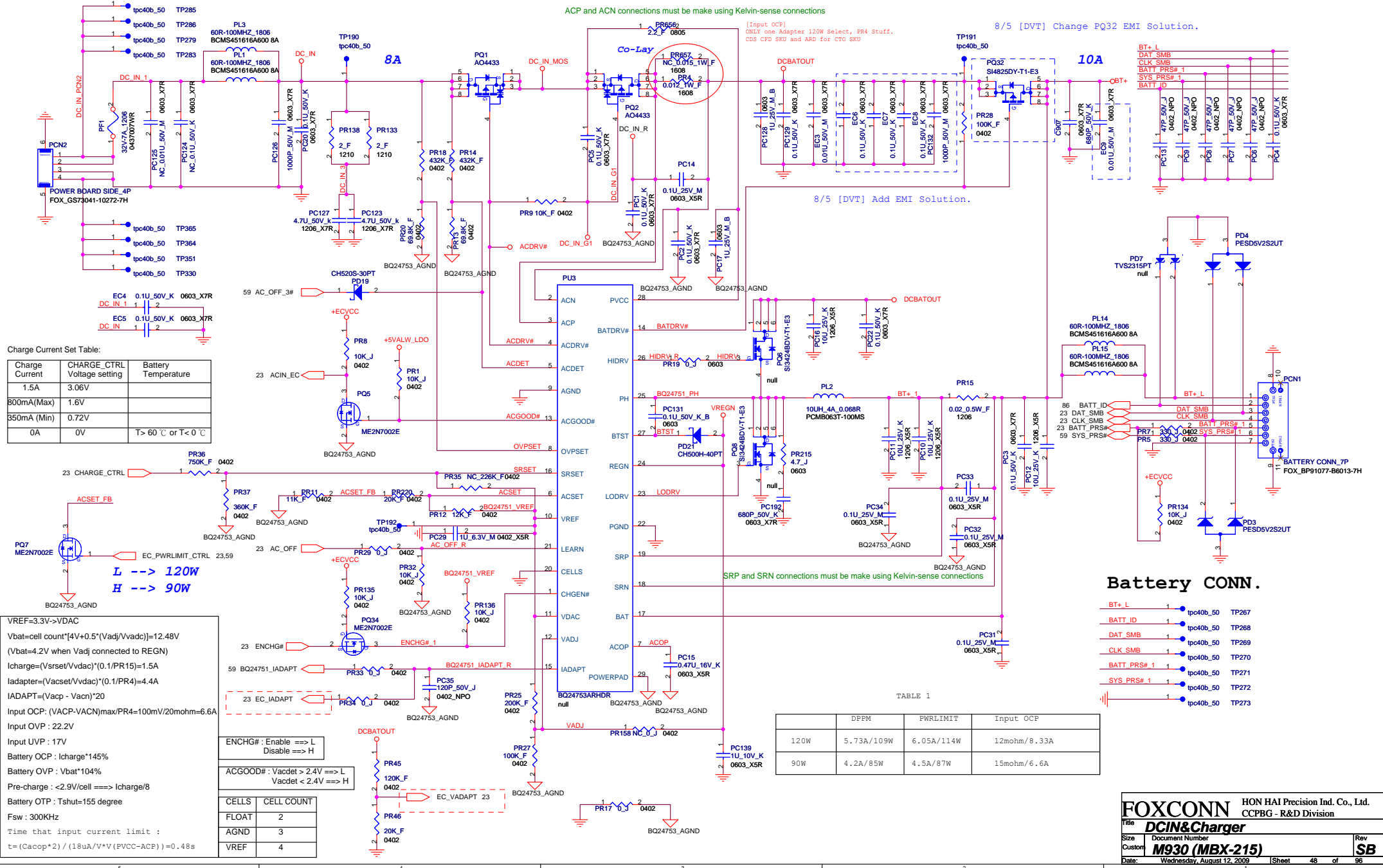
System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
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N-Channel transistor
+1_8VRUN/2A
APL5912 LDO
+1_5VRUN/4A
N-Channel transistor
+1_5VSUS/14A
N-Channel transistor
+0_75VRUN/2A
APL9513 LDO
PEX_VDD/2.5A
+5VALW_LDO
AT5208 LDO
+ECVCC/100mA
+12V For Load switch
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

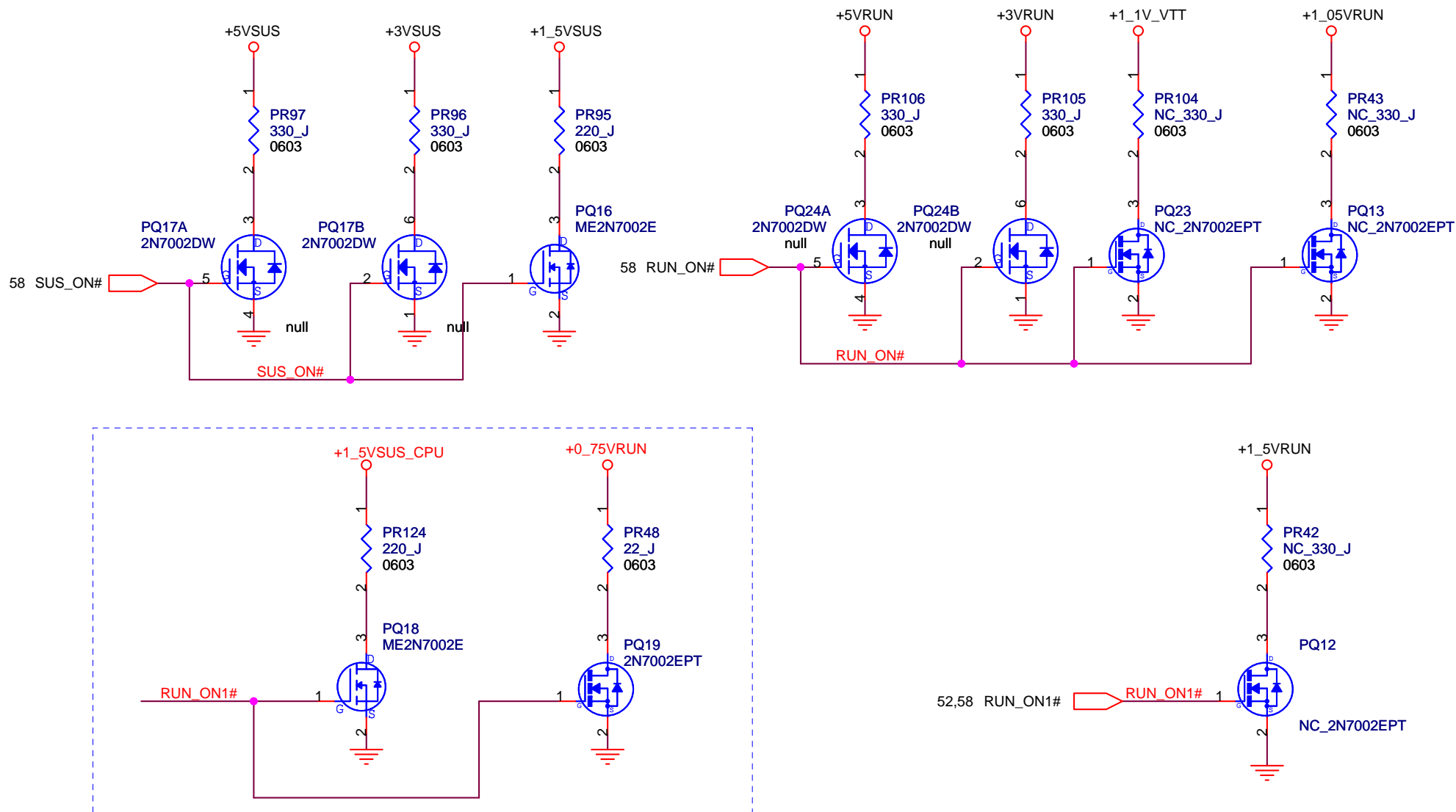
System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
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N-Channel transistor
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APL5912 LDO
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+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
+3VSUS/1.5A
N-Channel transistor
+3VRUN/5A
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+1_5VSUS/14A
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APL9513 LDO
PEX_VDD/2.5A
+5VALW_LDO
AT5208 LDO
+ECVCC/100mA
+12V For Load switch
+1_1V_VTT/15A
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+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
+3VSUS/1.5A
N-Channel transistor
+3VRUN/5A
N-Channel transistor
+1_8VRUN/2A
APL5912 LDO
+1_5VRUN/4A
N-Channel transistor
+1_5VSUS/14A
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APL9513 LDO
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+ECVCC/100mA
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+1_1V_VTT/15A
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+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A

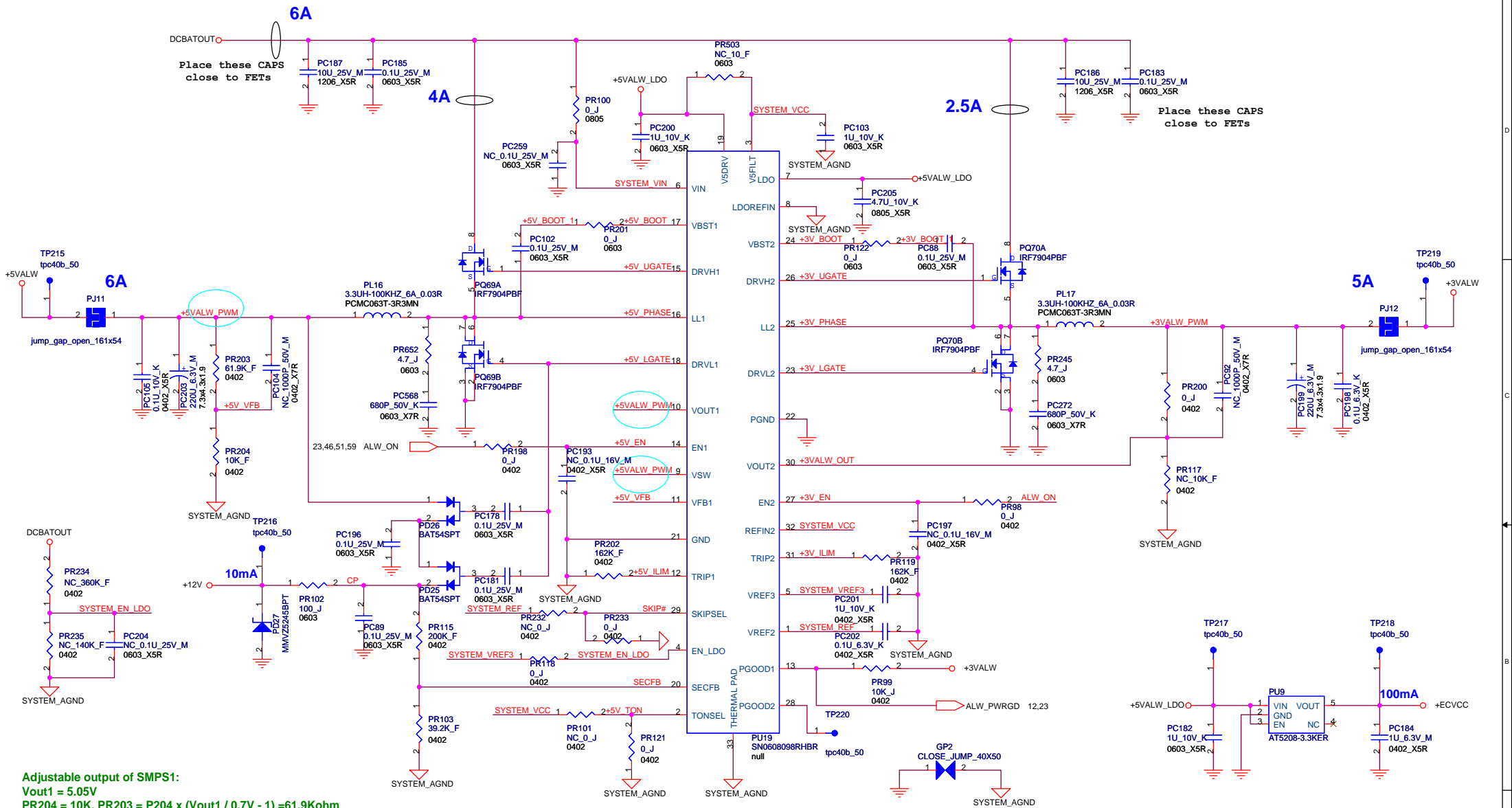
System
+5VALW/6A
N-Channel transistor
+5VSUS/0.6A
N-Channel transistor
+5VRUN/4.5A
N-Channel transistor
+3VALW/5A
N-Channel transistor
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+1_8VRUN/2A
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+12V For Load switch
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A
+1_1V_VTT/15A
+1_05RUN/5A





7/24 [DVT] INTEL S3 Power Reduction Solution.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title DISCHARGE CIRCUIT			
Size A	Document Number M930 (MBX-215)		Rev SB
Date:	Wednesday, August 12, 2009	Sheet 49 of	96



Adjustable output of SMPS1:
 Vout1 = 5.05V
 PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) = 61.9Kohm

Second Feedback :
 Vout_sec = 12V, PR103 = 20Kohm
 PR115 = PR103 x (Vout_sec / 2V - 1) = 100Kohm

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT (VIN - VOUT) / (VIN * f * LIR * ILOAD (MAX))$$

$$Rocp = (Iocp - Irripple / 2) * (10 * Rds (on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * VFB1$$

Current limit resistor for SMPS1 :
 Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
 PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
 Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
 PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

7/29 [DVT] Change PR123 to 1kOhm.

7/30 [DVT] PWM setting adjust

7/8 [DVT] OCP setting adjust

Sense line are 18mil wide

4/23 Change the logic design for MOR request
(low enable voltage concern)

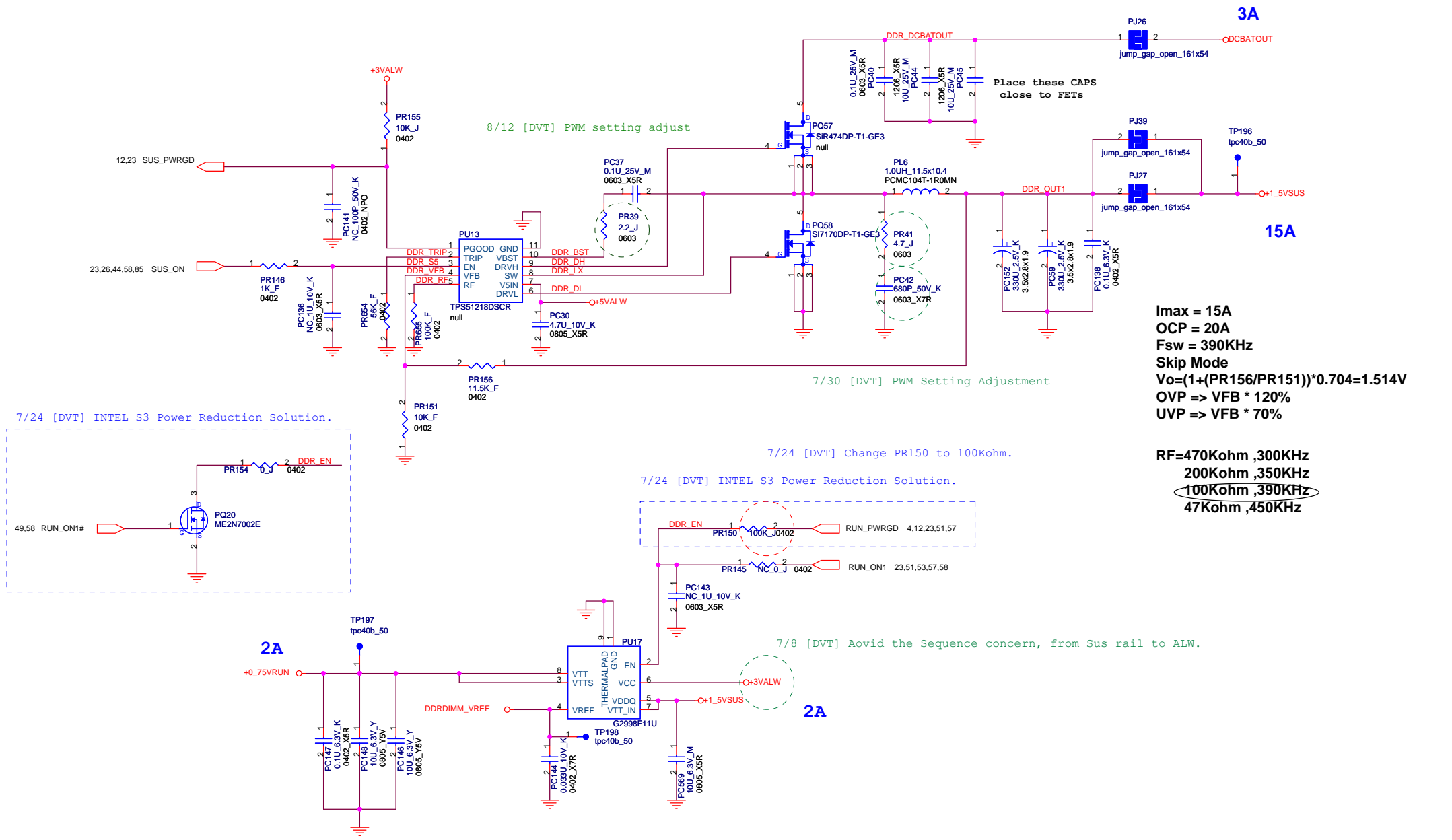
7/29 [DVT] Change PR160 to 1kOhm.

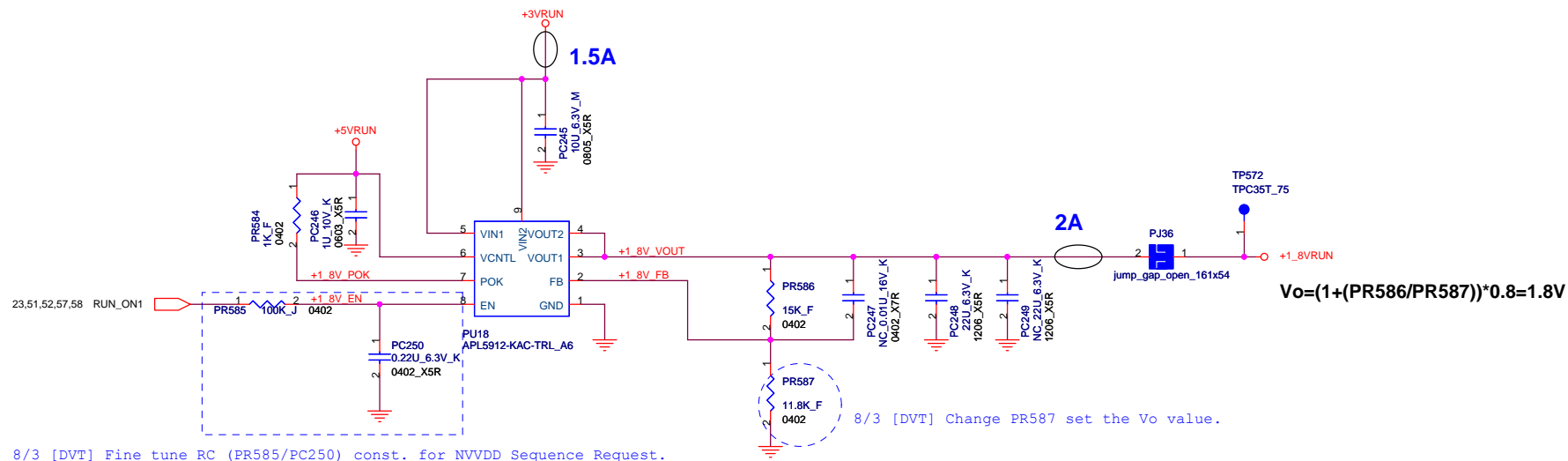
4/27 Revise the resistor divider value of PR505 and PR506.

Imax = 15A
OCP = 20A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR187/PR208)) * 0.704 = 1.05V$
 $V_o = (1 + (PR187/(PR208/PR590))) * 0.704 = 1.1V$
OVP => VFB * 120%
UVP => VFB * 70%
CF 0 1.1 V
AR 1 1.05 V

RF = 470Kohm , 300KHz
200Kohm , 350KHz
100Kohm , 390KHz
47Kohm , 450KHz

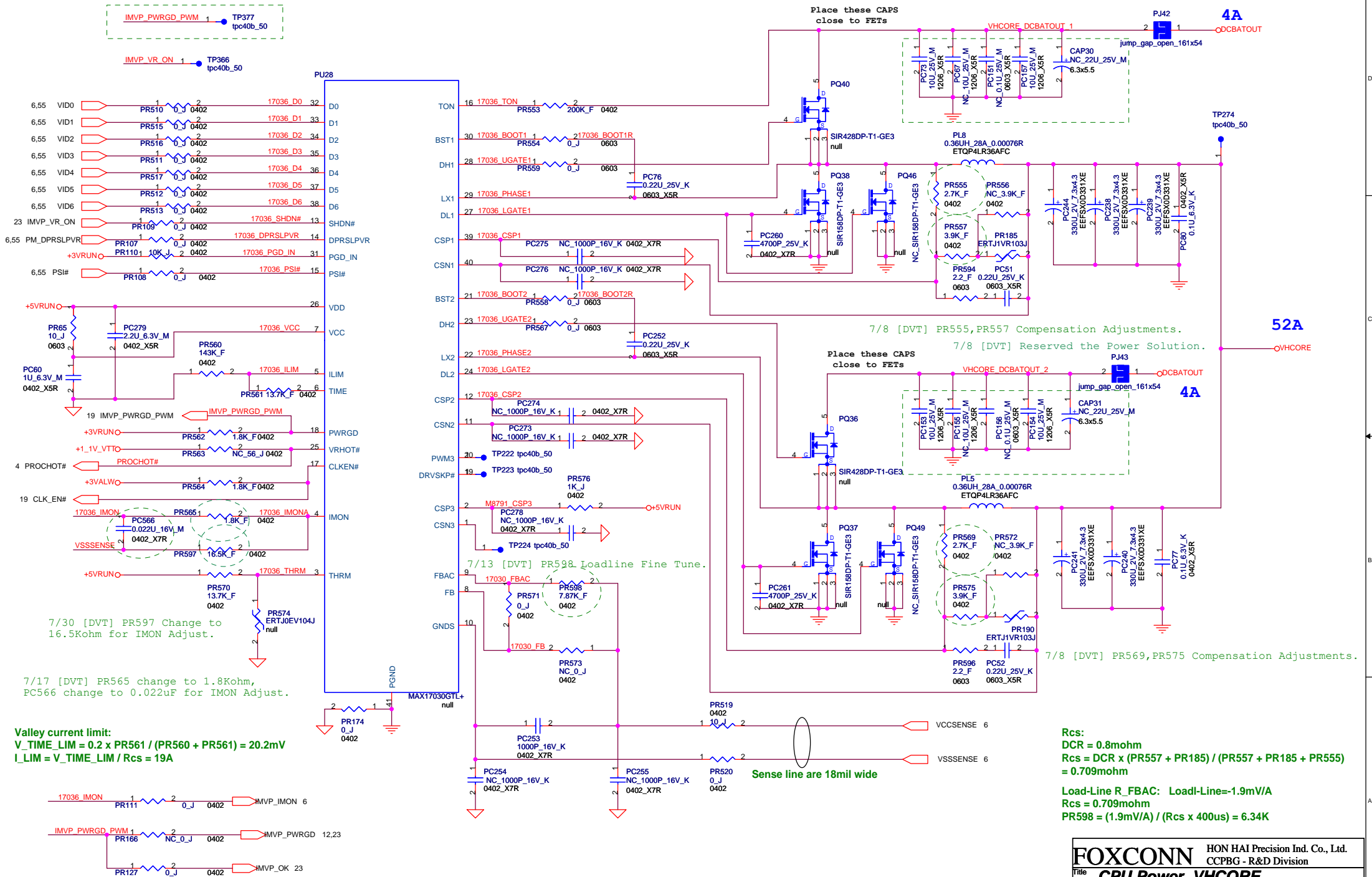
Imax = 5A
OCP = 7A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR505/PR506)) * 0.704 = 1.05V$
OVP => VFB * 120%
UVP => VFB * 70%





7/13 [DVT] For L6 Power Test Station usage (Top-side)

7/8 [DVT] Reserved the Power Solution.

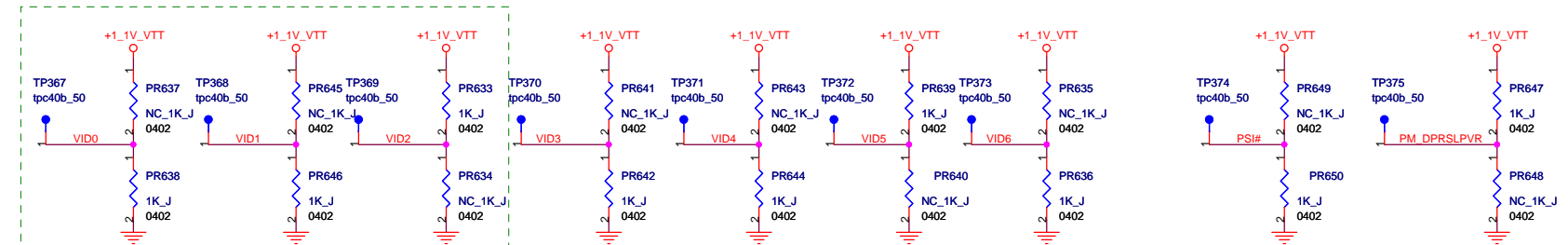
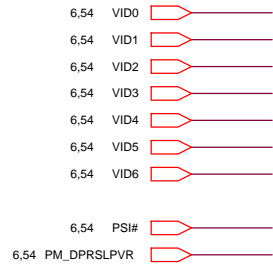


Rcs:
 $DCR = 0.8mohm$
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm$
Load-Line R_FBAC: Load-Line = -1.9mV/A
 $Rcs = 0.709mohm$
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$

Default value of VID [6:0] = [0100100] , PSI# = 0 , PROC_DPRS LPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)

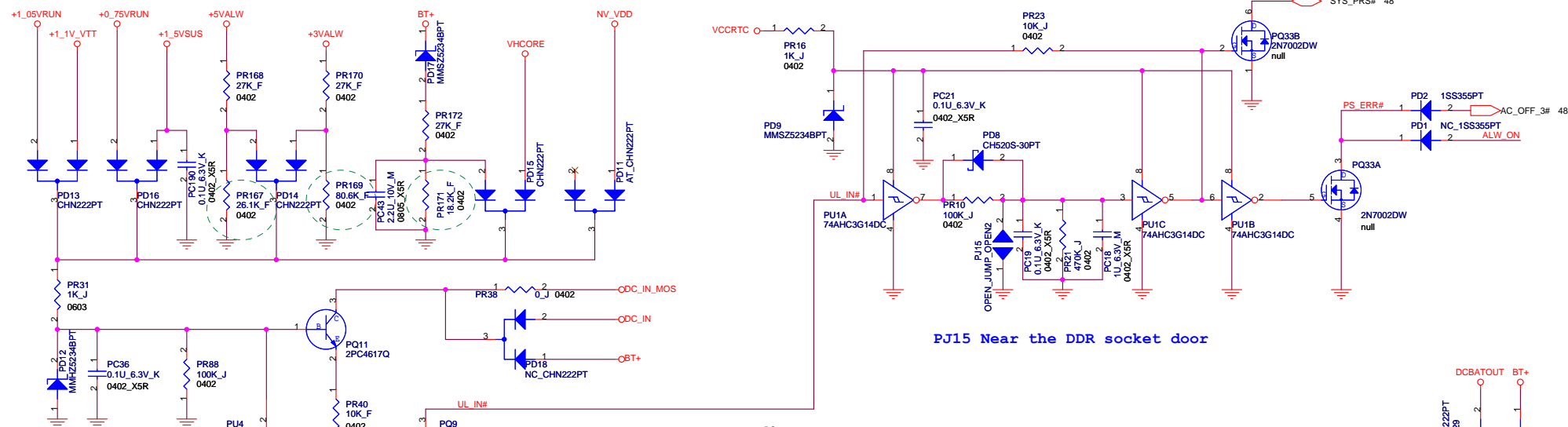
- 416056_416056_Ard_EDS_Rev.1.1
- 403779_Clarksfield_MPG_Rev1.5



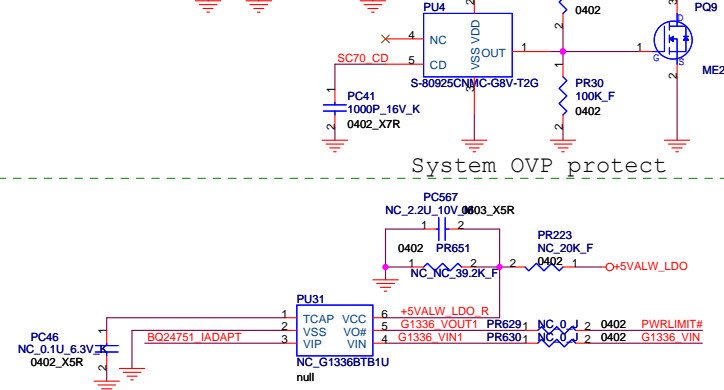
7/8 [DVT] Follow the ARD/CFD EDS Setting to set as SV type.

Delete iGPU Path on DVT for Cost Down

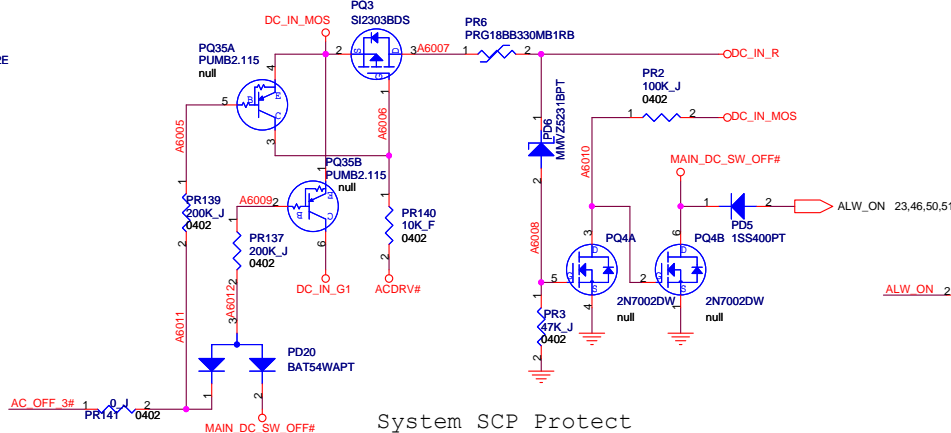
7/17 [DVT] PR167 change to 26.1Kohm, PR169 change to 80.6Kohm ,PR171 change to 18.2Kohm for OVP Adjust.



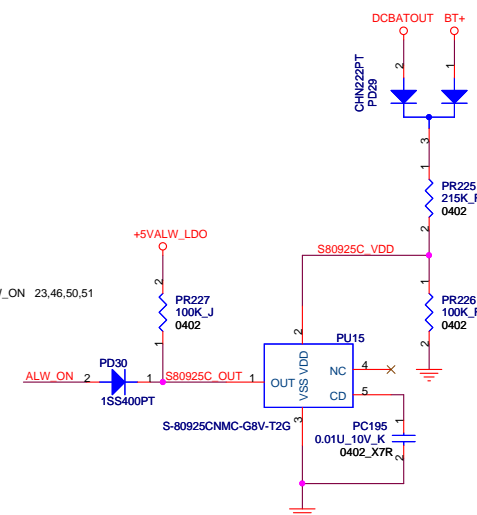
PJ15 Near the DDR socket door



System OVP protect

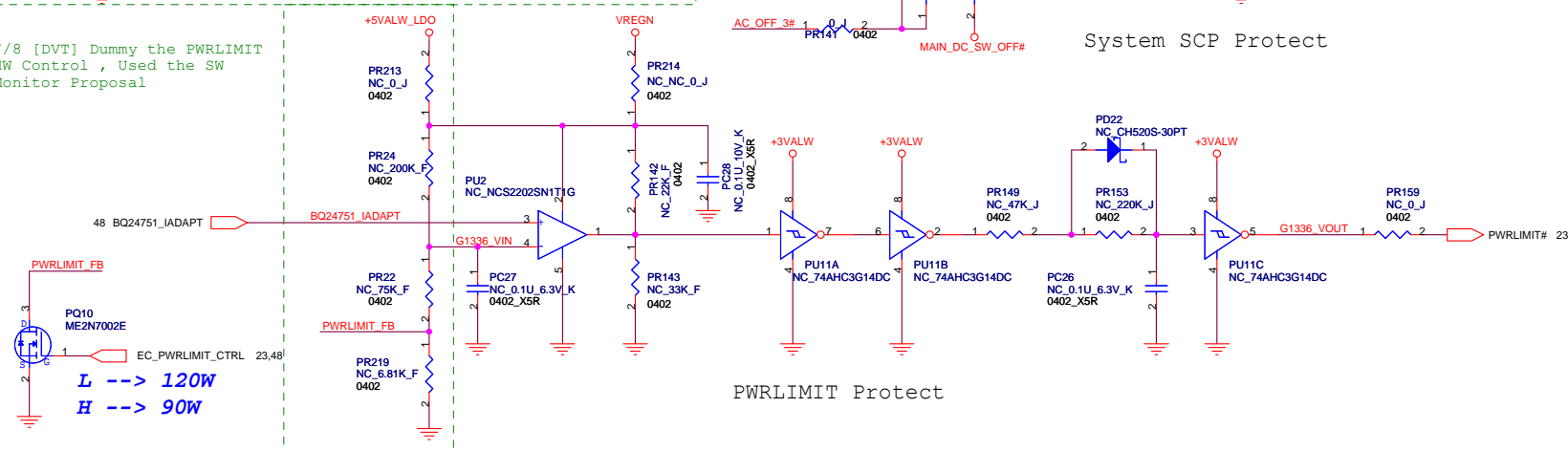


System SCP Protect



Battery UVP Protect

7/8 [DVT] Dummy the PWRLIMIT
HW Control , Used the SW
Monitor Proposal



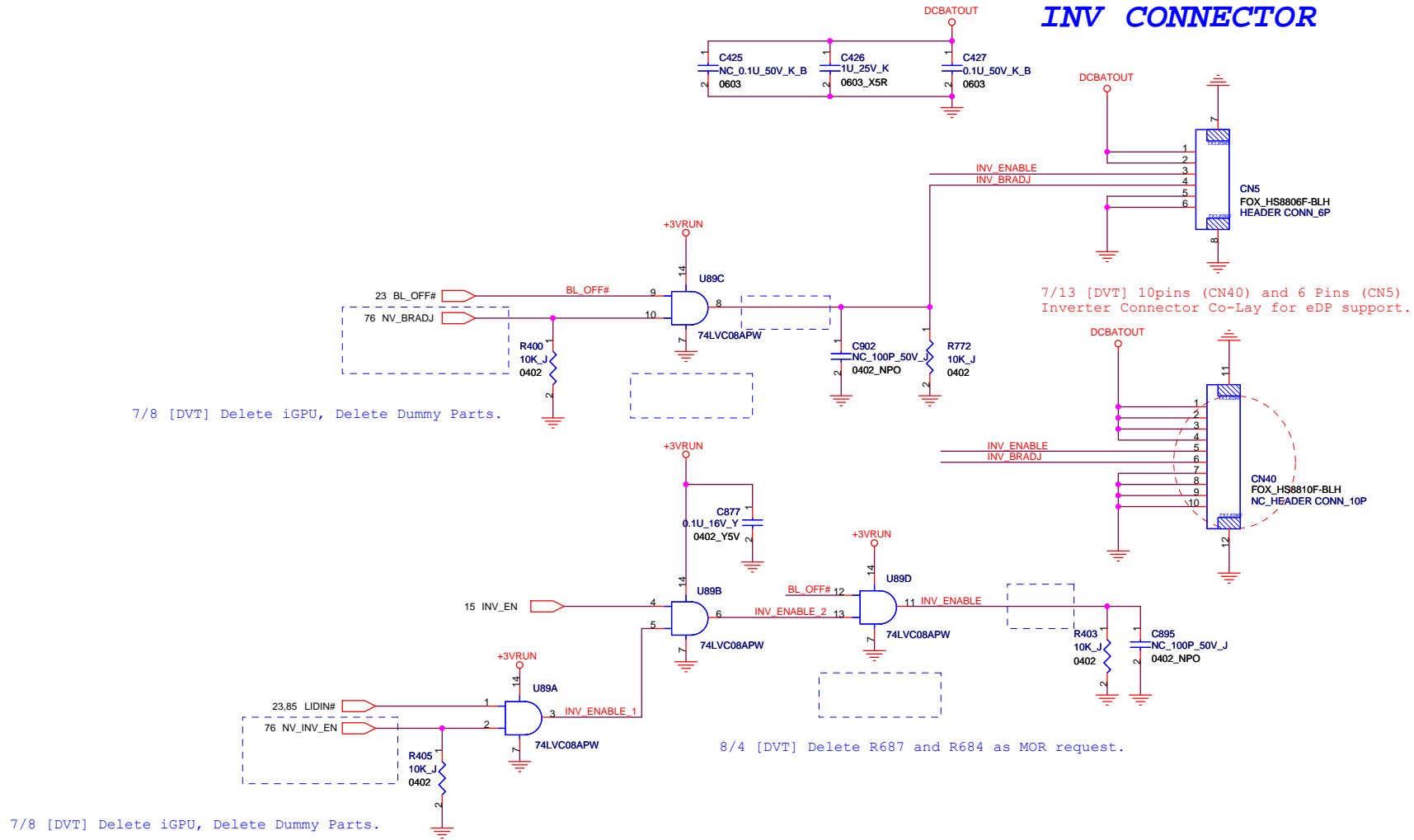
PWRLIMIT Protect

VIINP	90W adaptor	120W adaptor
PWRLIMIT	4.5A 87W	6.05A 114W

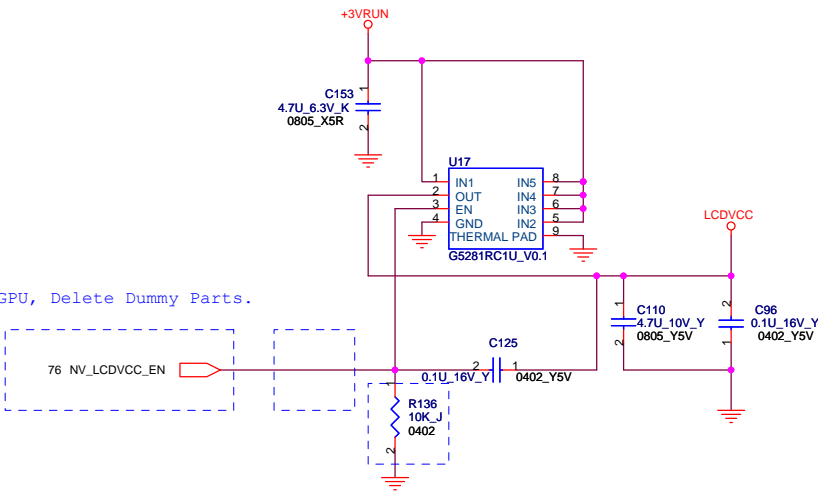
```
adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax
```

$L \rightarrow 120W$
 $H \rightarrow 90W$

INV CONNECTOR



LCDVCC Power

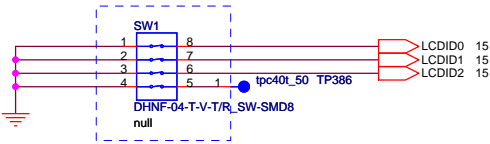


7/8 [DVT] Delete iGPU, Delete Dummy Parts.

7/15 [DVT] Delete U46 to fix the DISPLAY OFF function issue.

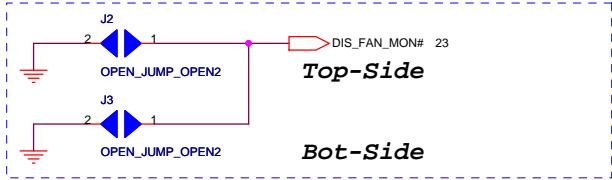
7/15 [DVT] Change R136 from 100Kohm to 10Kohm.

PANEL ID

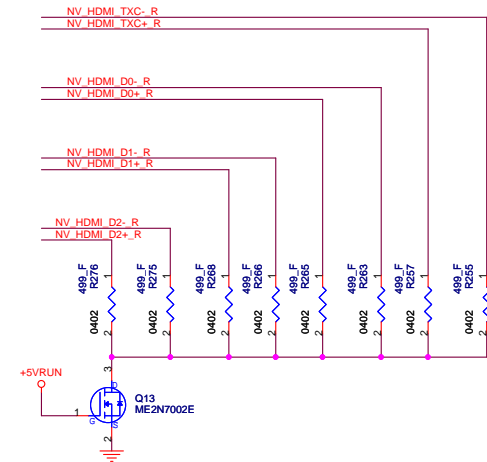
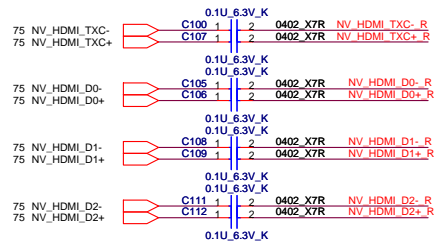


SW1 (Panel ID)	LCDID2	LCDID1	LCDID0
CRT (No LCD)	0	0	0
EW1 (Sharp)	0	0	1
EW1 (AUO)	0	1	0
EW1 (LGD)	0	1	1
EW3 (Sharp)	1	0	0
RESERVED	1	0	1
RESERVED	1	1	0
RESERVED	1	1	1

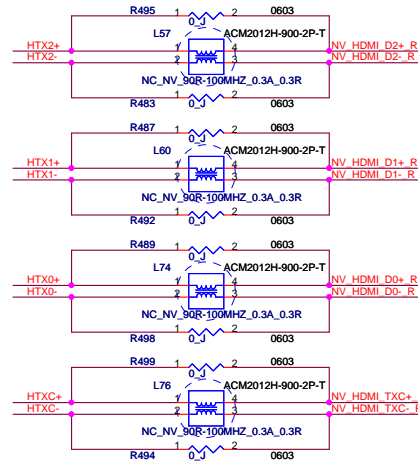
ON:0 , OFF:1



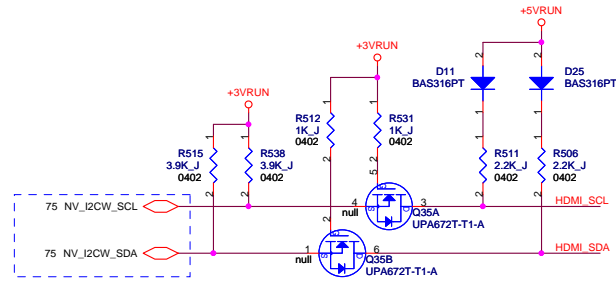
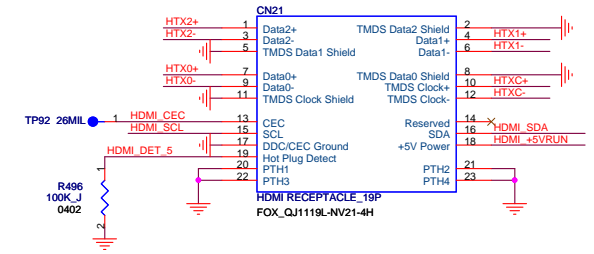
DIS_FAN_MON# for L6 BFT Test



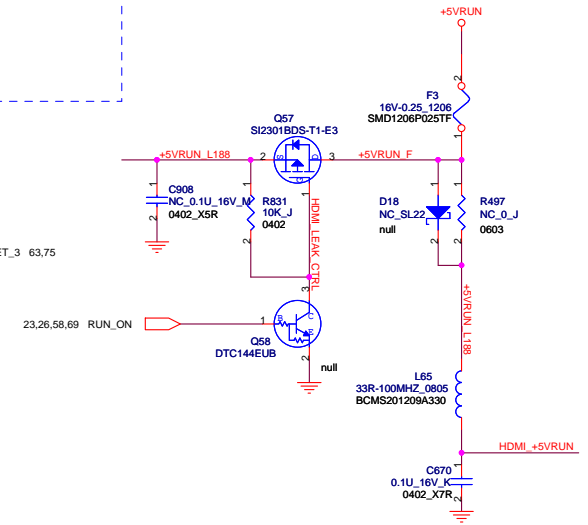
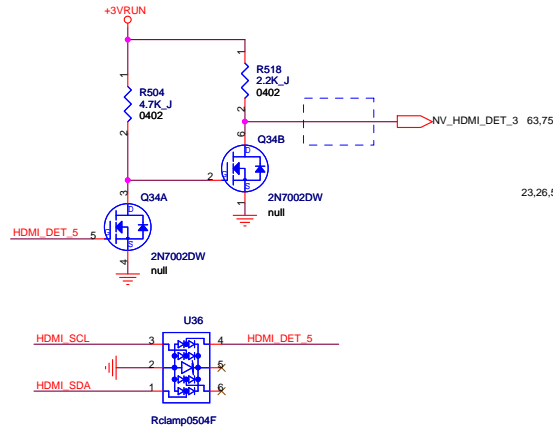
Data line capacitance to GND need less than 10pF,
so those parts need close to HDMI connector



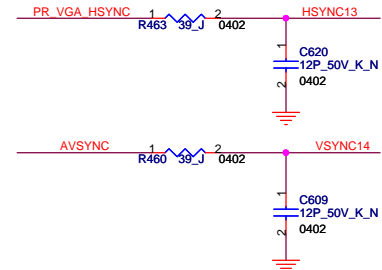
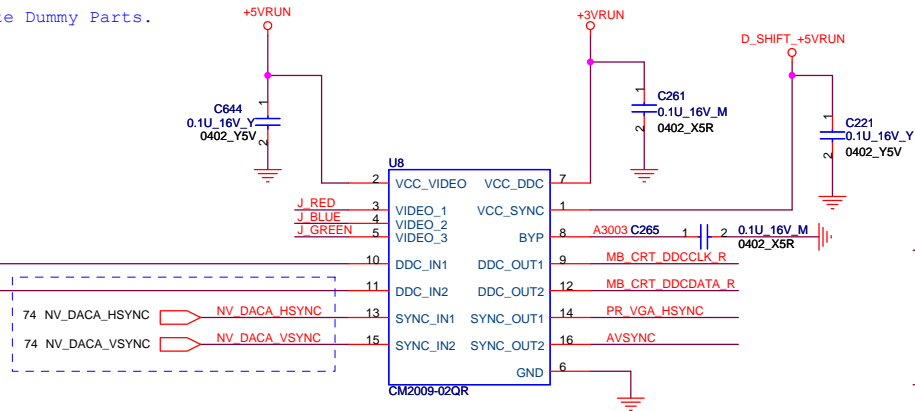
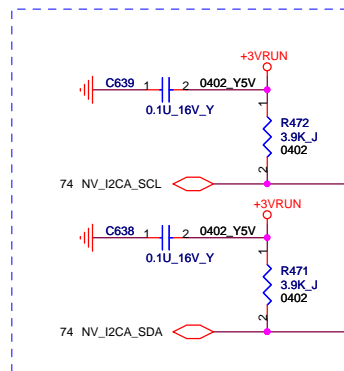
7/8 [DVT] Delete iGPU, Delete Dummy Parts.



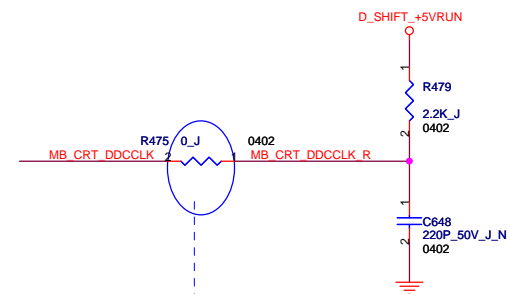
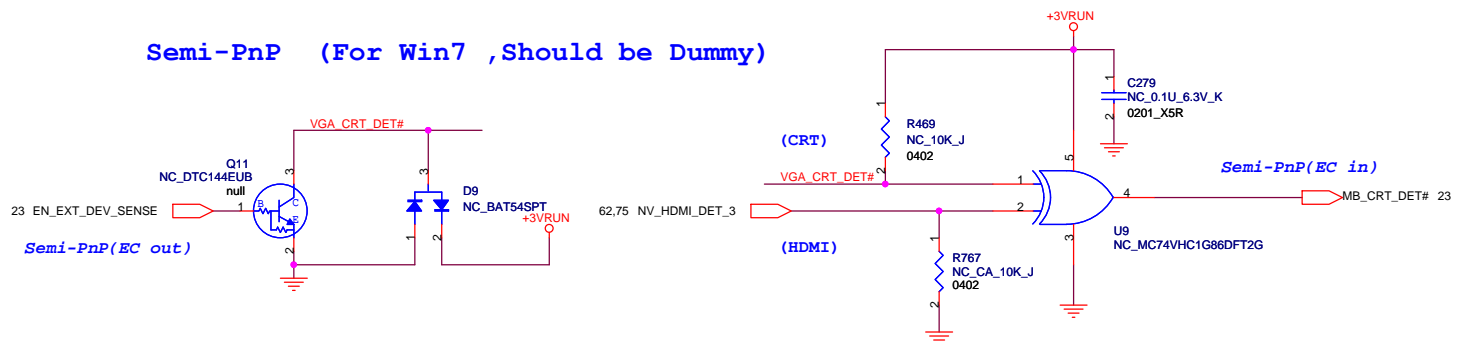
7/8 [DVT] Delete iGPU, Change the Net name.



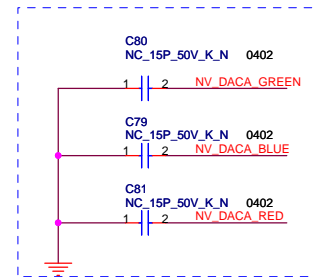
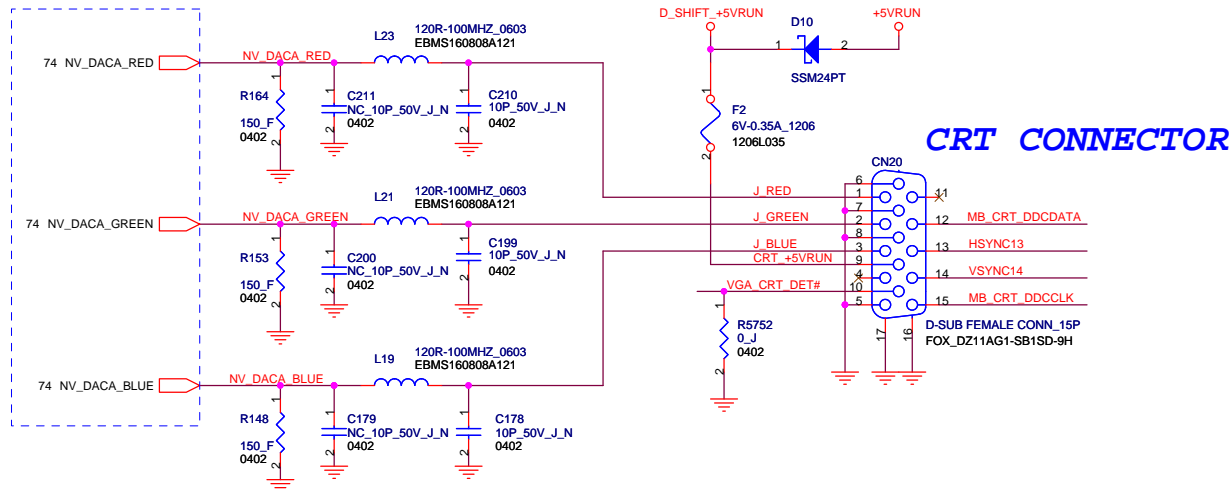
7/8 [DVT] Delete iGPU, Delete Dummy Parts.



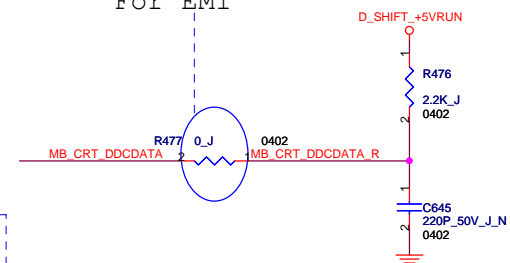
Semi-PnP (For Win7 ,Should be Dummy)



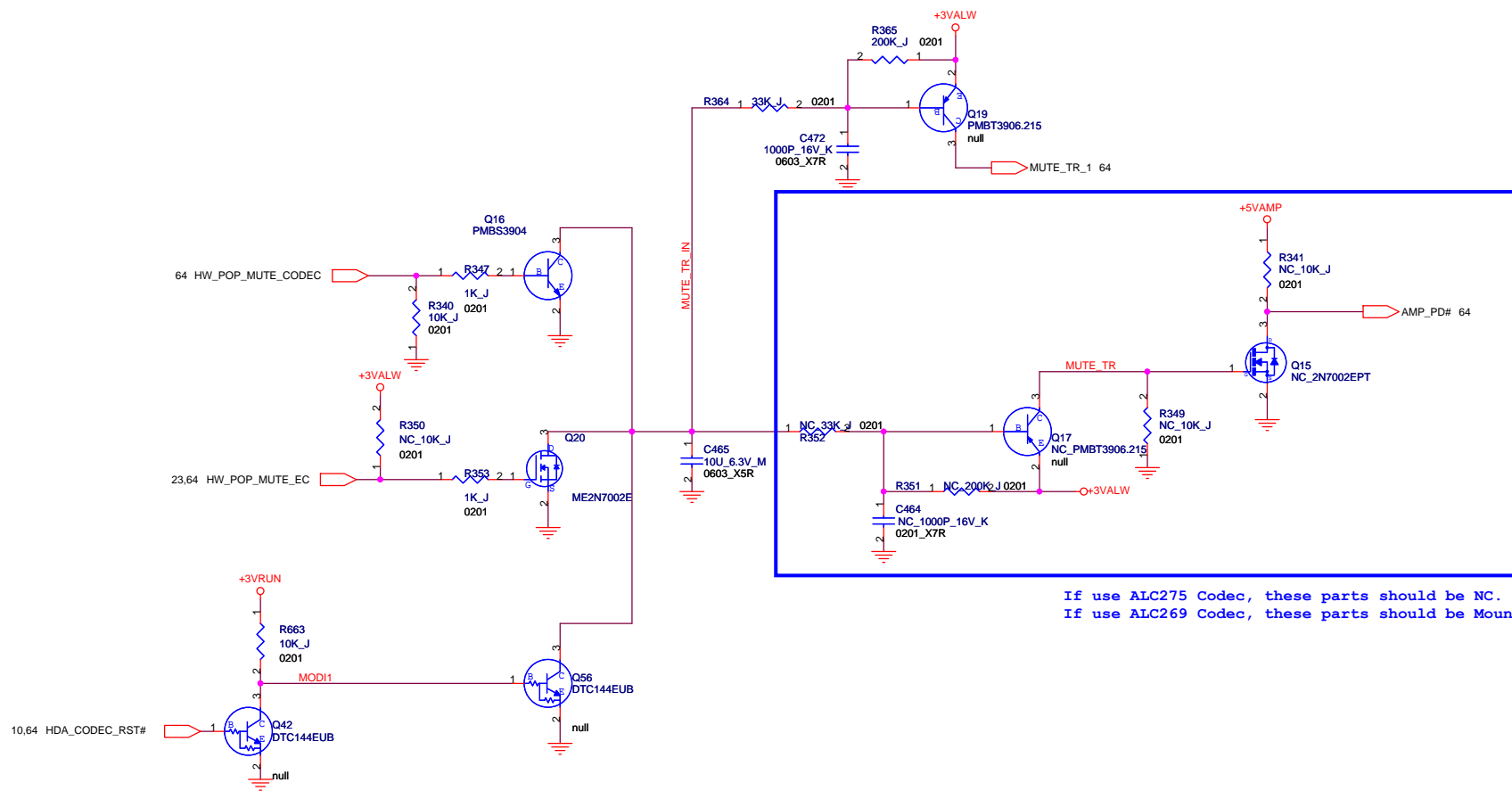
7/8 [DVT] Delete iGPU, Change Net name.



For EMI

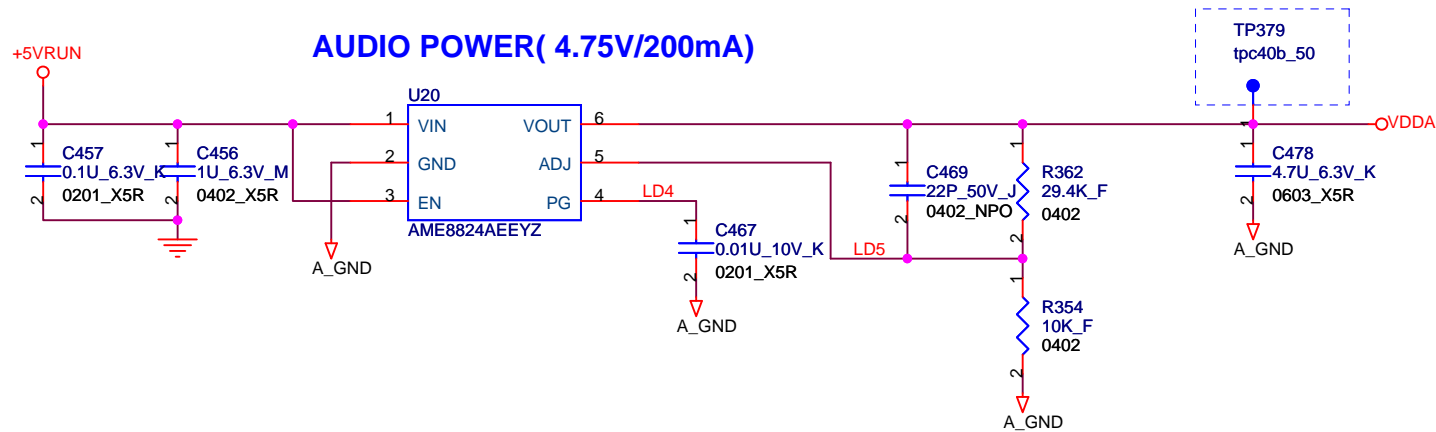


7/8 [DVT] Delete iGPU, Change Net name.



If use ALC275 Codec, these parts should be NC.
If use ALC269 Codec, these parts should be Mount.

7/13 [DVT] Add Test Point TP379



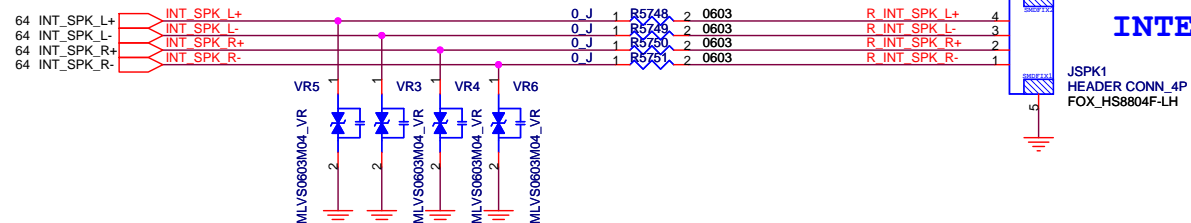
Delete Class D Amp. when implemented ALC275.

TP114 tpc40t_50 1 R_INT_SPK L+

TP117 tpc40t_50 1 R_INT_SPK L-

TP116 tpc40t_50 1 R_INT_SPK R+

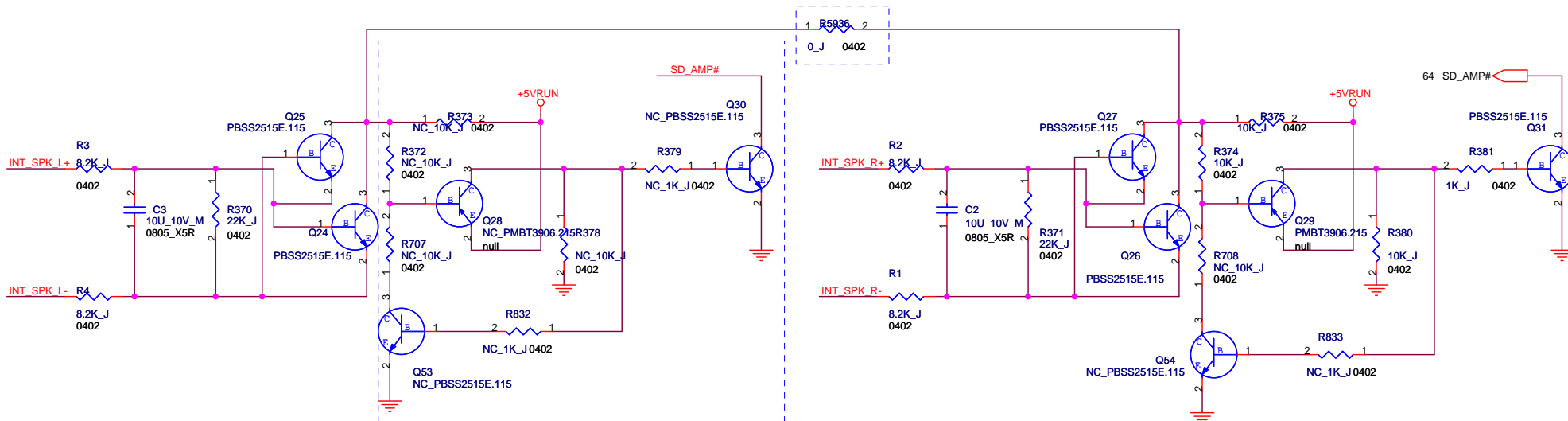
TP115 tpc40t_50 1 R_INT_SPK R-



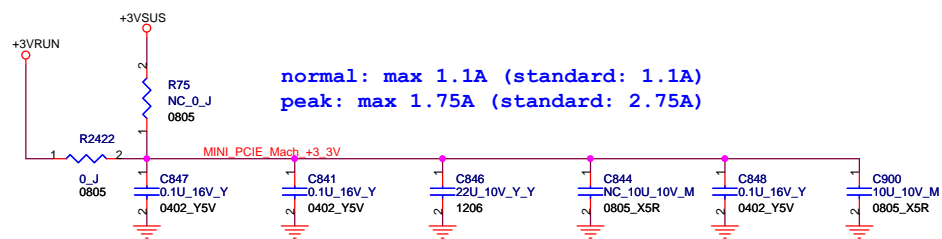
INTERNAL SPEAKER

8/10 [DVT] Reserve the L-ch parts and add R5936 for C/D as MOR request.

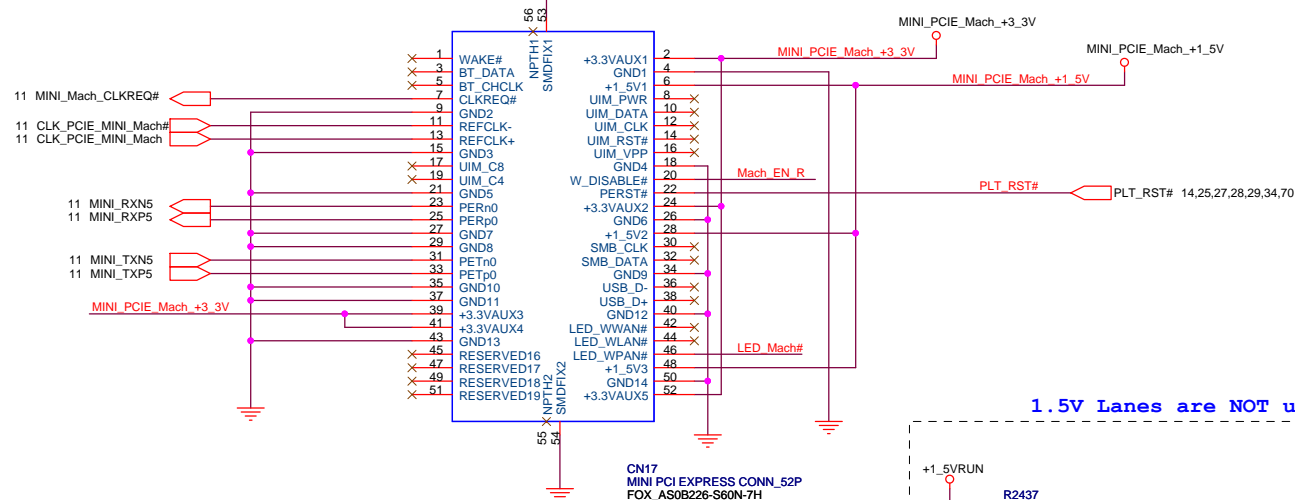
For Shut-down Codec Amp. power (PVDD1 and PVDD2)



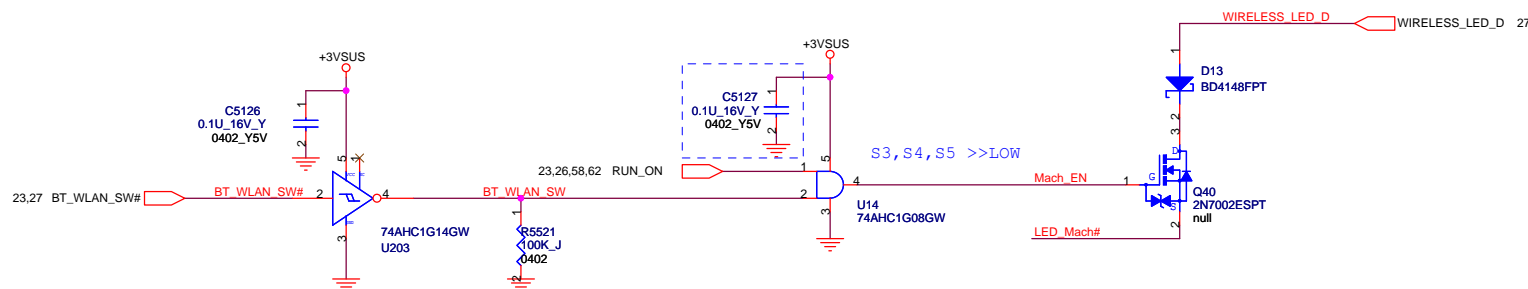
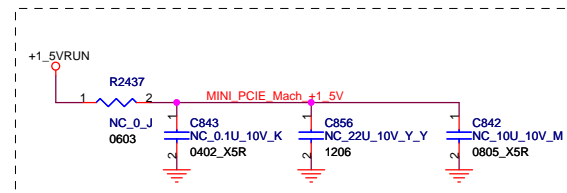
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size		Document Number	
B		M930 (MBX-215)	
Date		Wednesday, August 12, 2009	
Sheet		68 of 96	
Rev		SB	



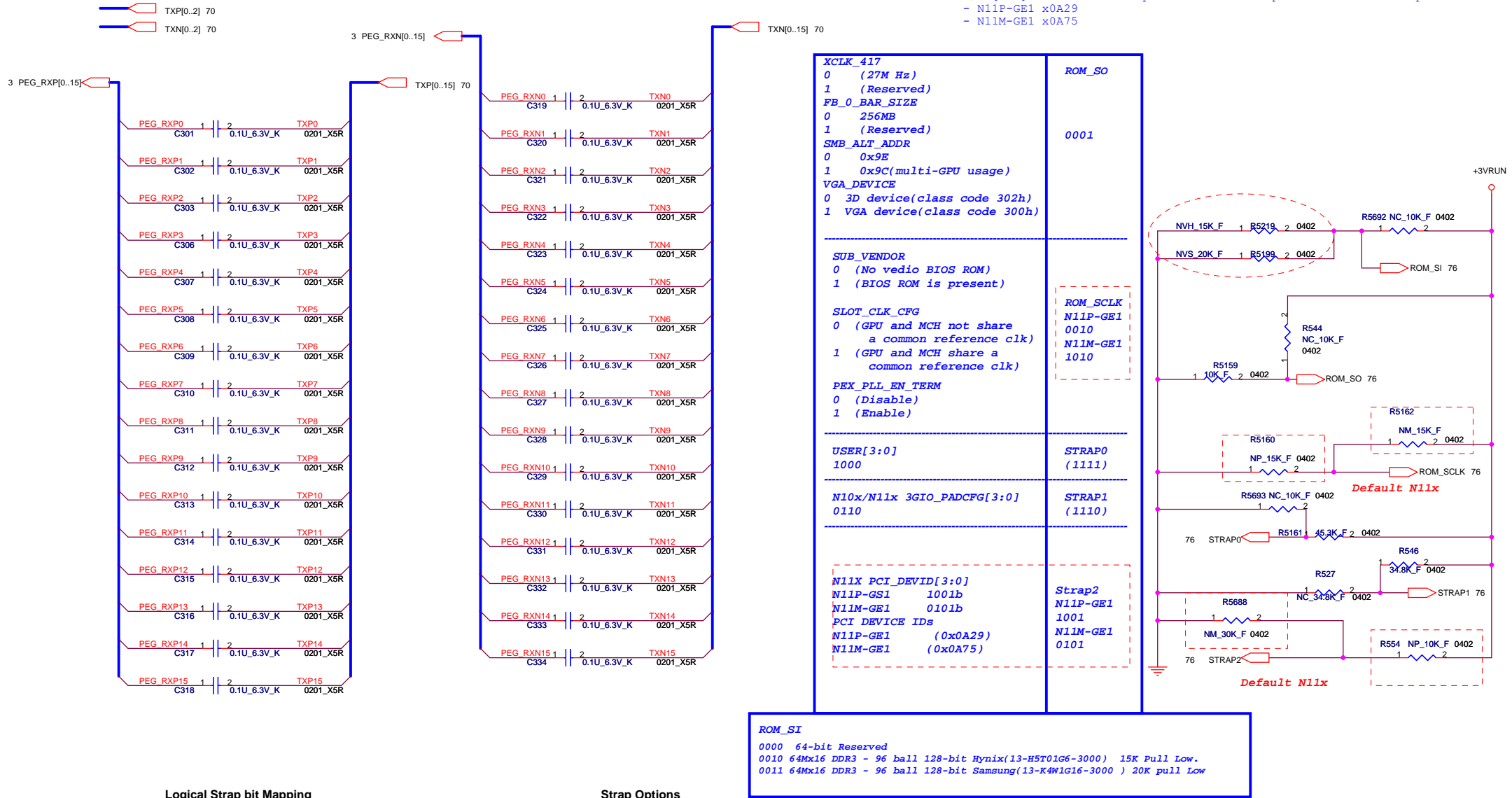
Mach CONN



1.5V Lanes are NOT used.



8/3 [DVT] Revise the Strap Pin value as FAEprovided for DVT Sample.
- N11P-GE1 x0A29
- N11M-GE1 x0A75



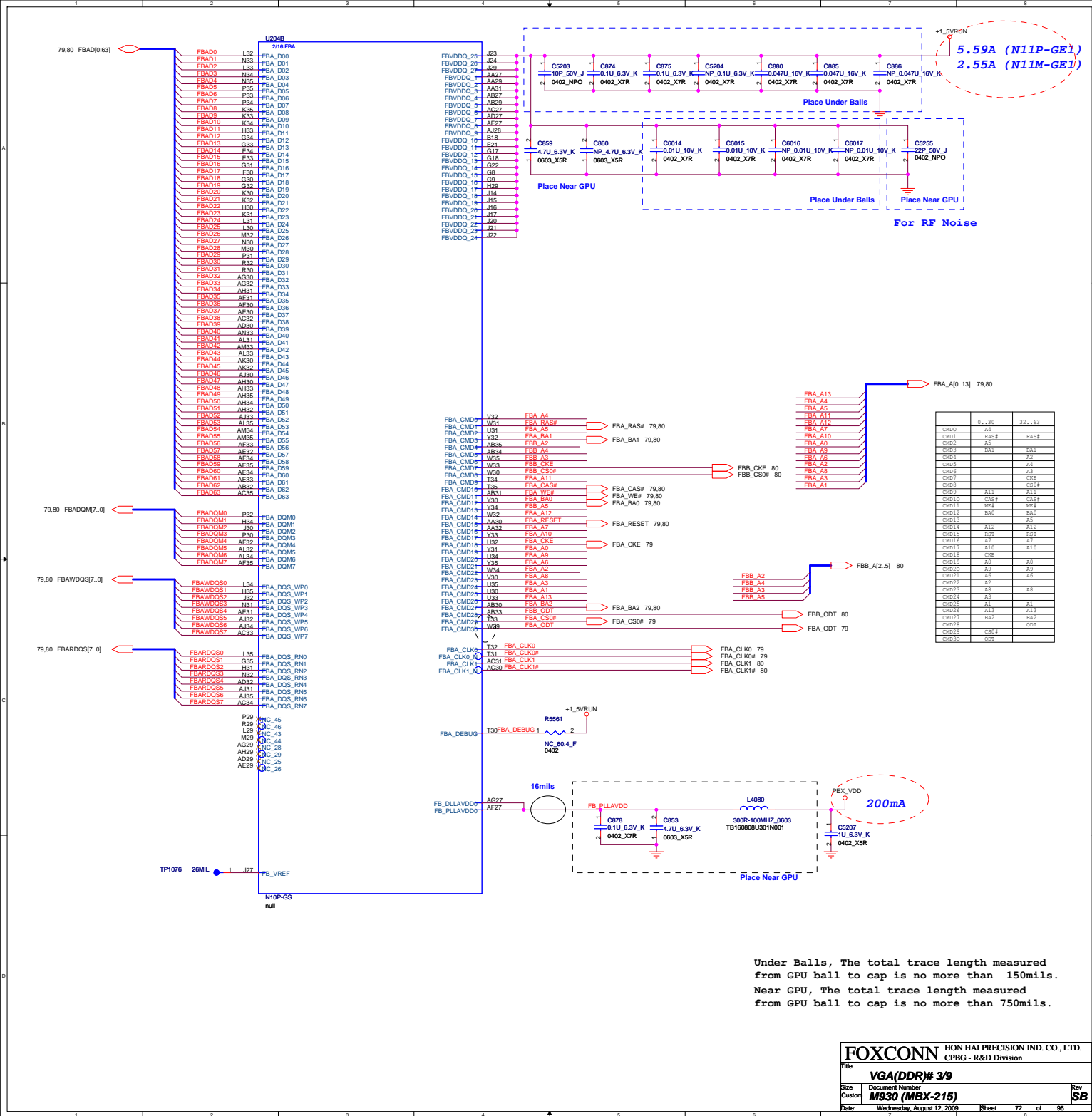
Logical Strap bit Mapping

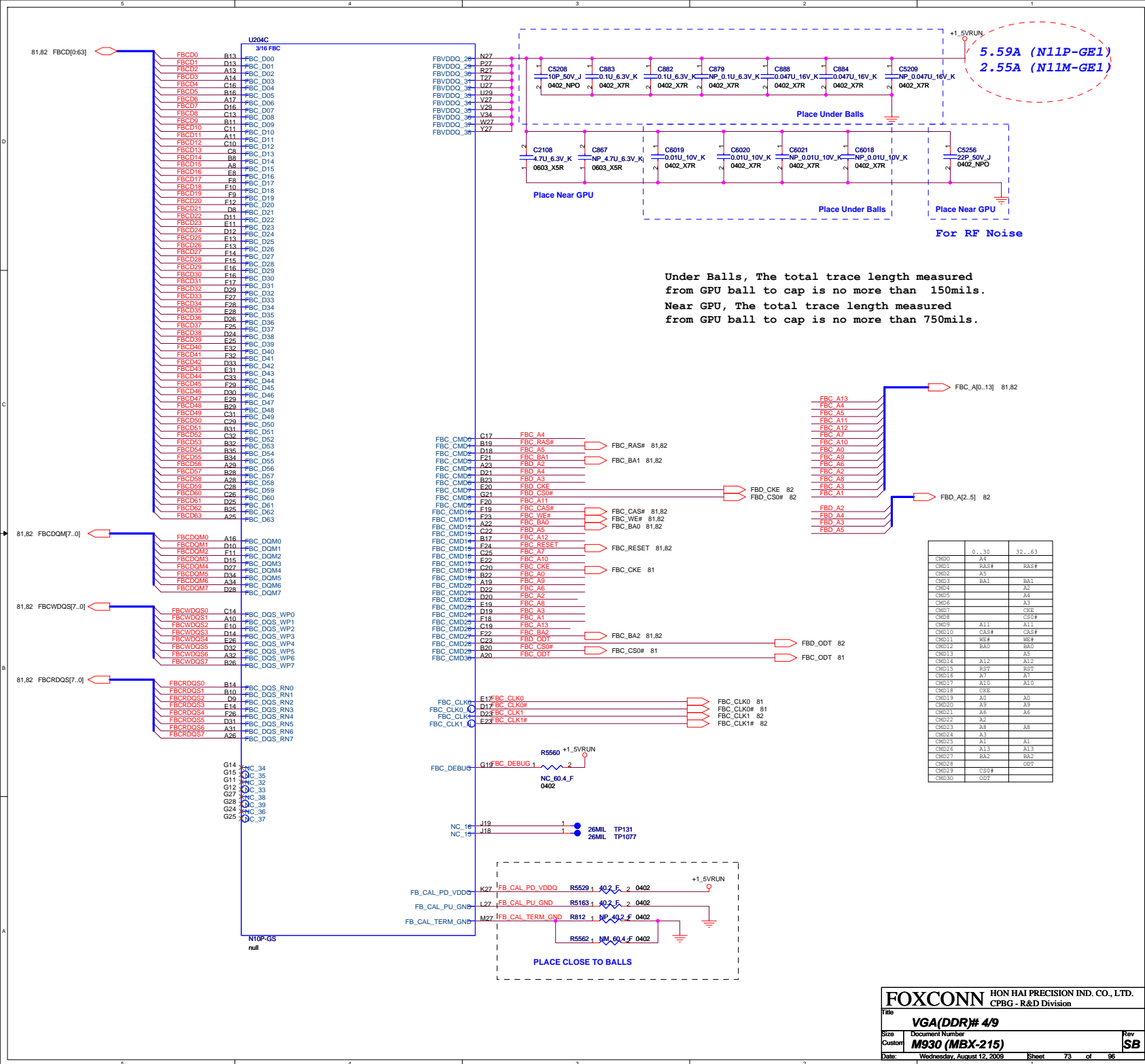
Resistor values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

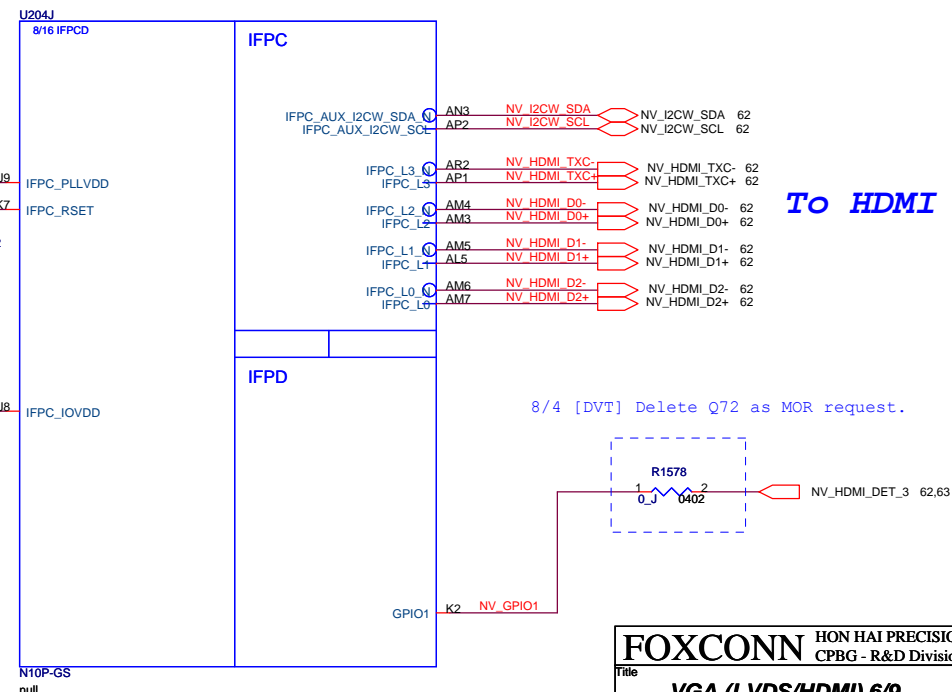
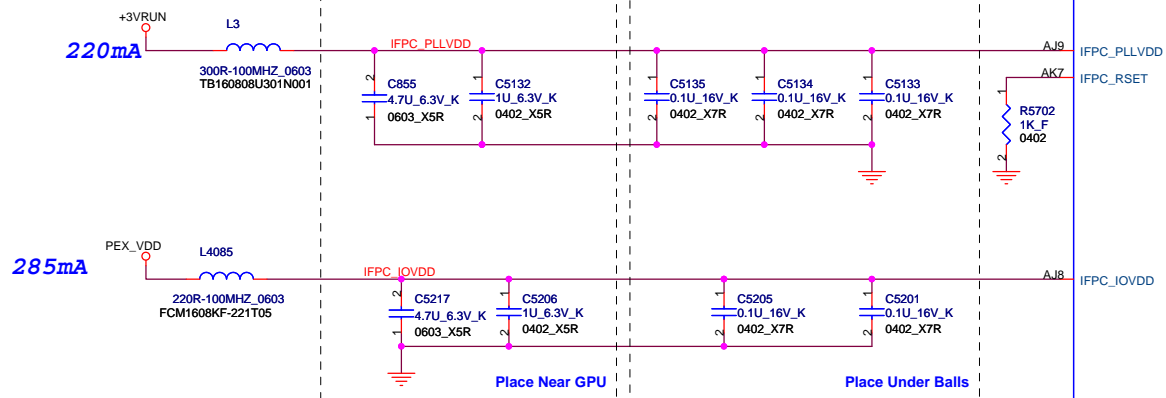
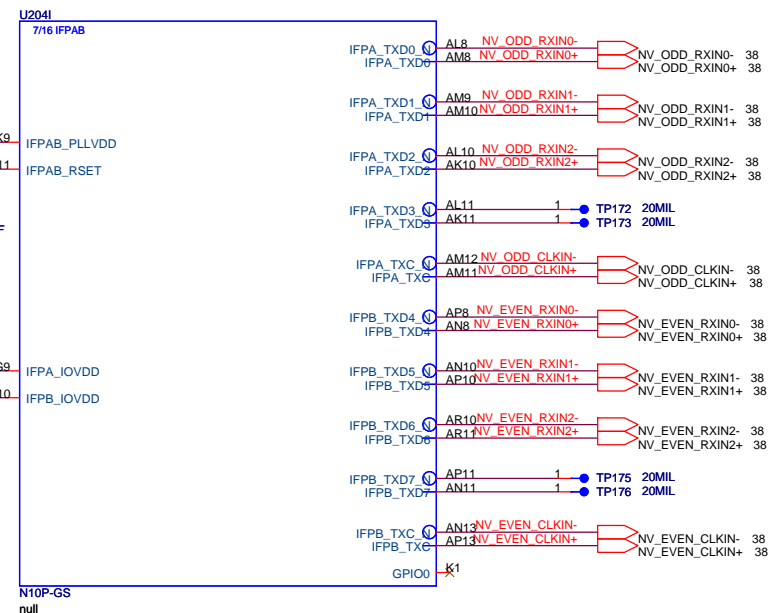
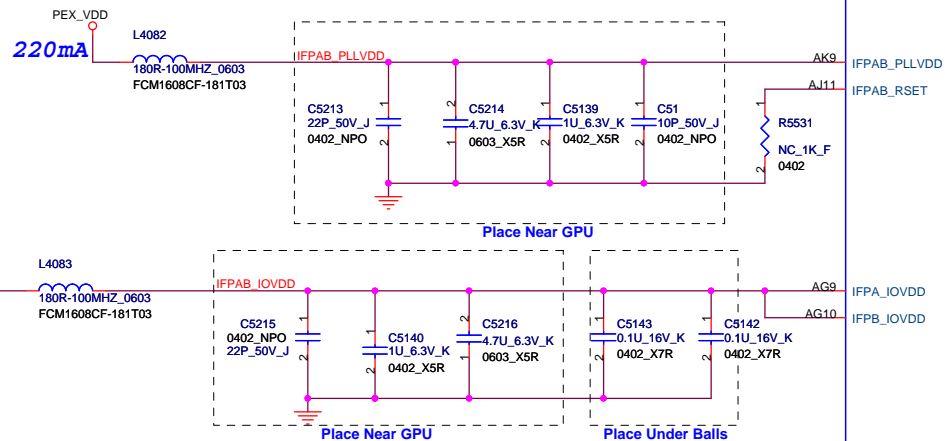
Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	BGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04202-001_v02_secured>

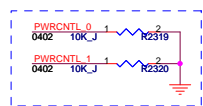
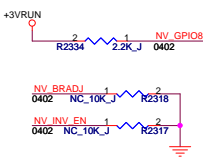
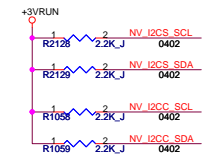
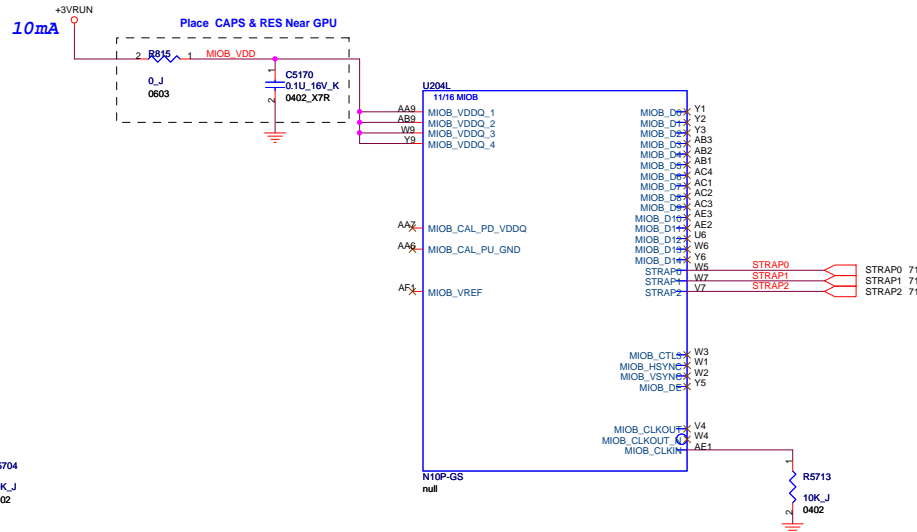
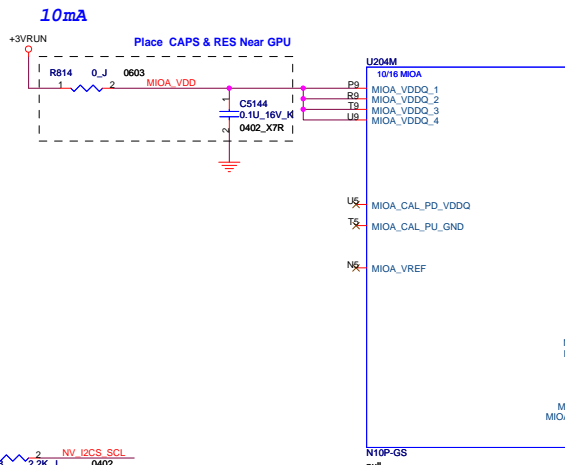
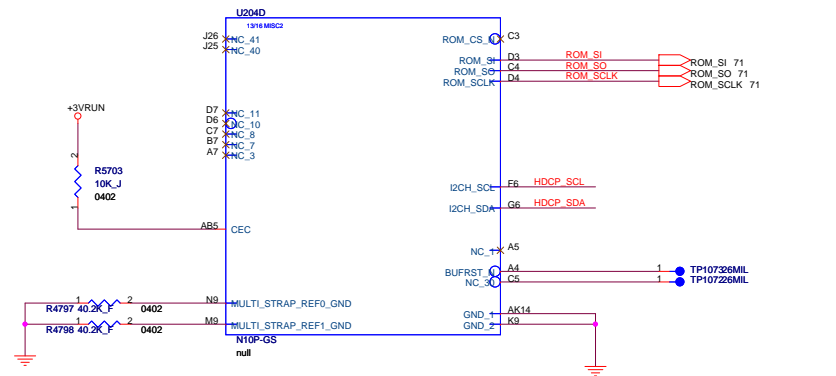
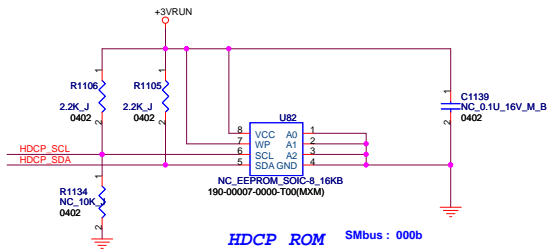




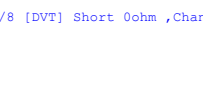


To HDMI CONN.

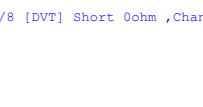
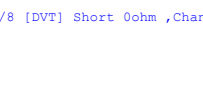
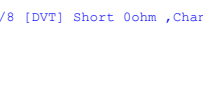
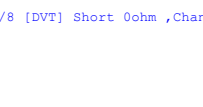
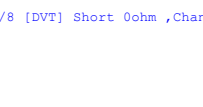
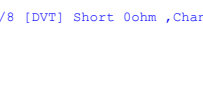
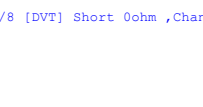
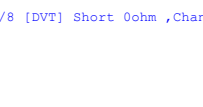
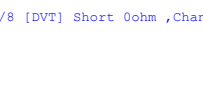
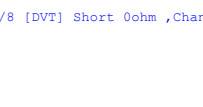
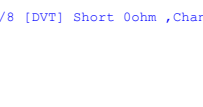
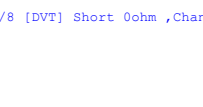
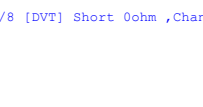
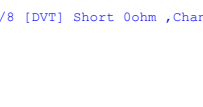
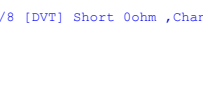
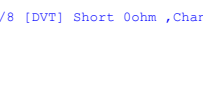
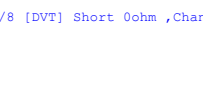
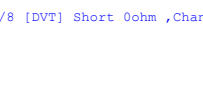
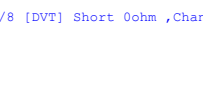
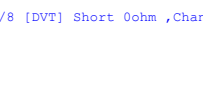
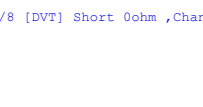
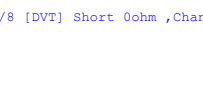
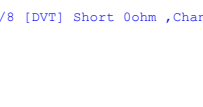
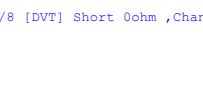
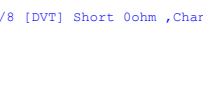
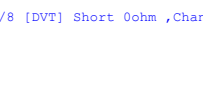
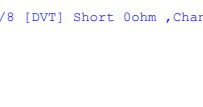
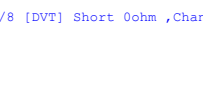
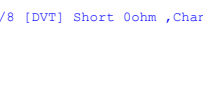
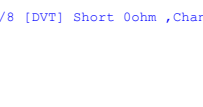
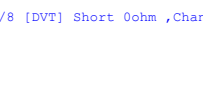
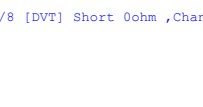
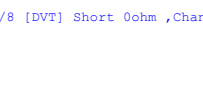
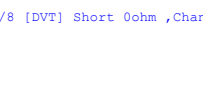
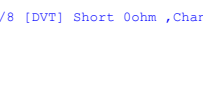
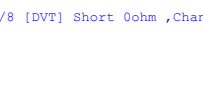
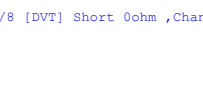
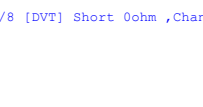
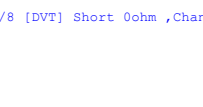
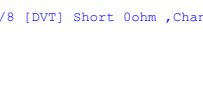
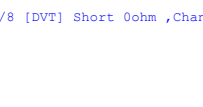
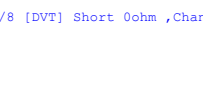
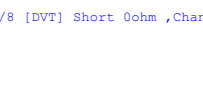
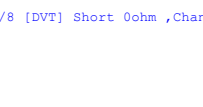
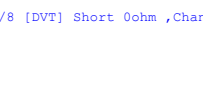
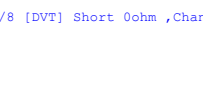
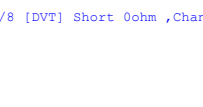
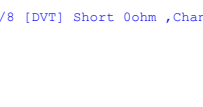
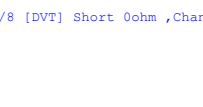
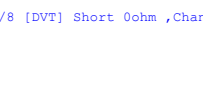
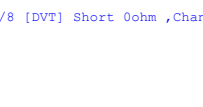
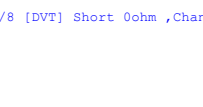
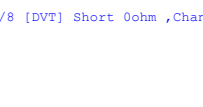
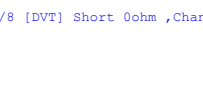
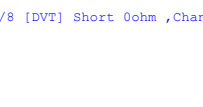
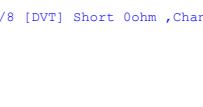
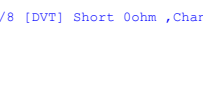
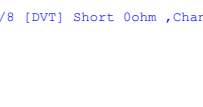
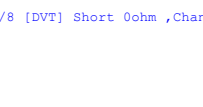
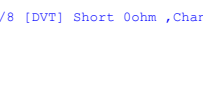
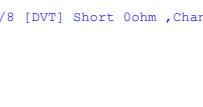
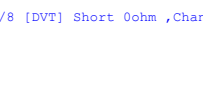
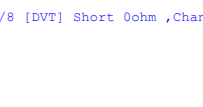
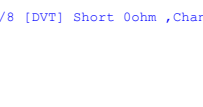
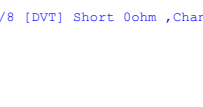
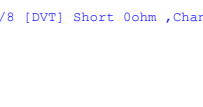
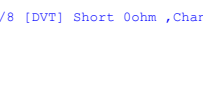
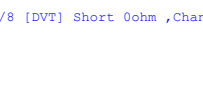
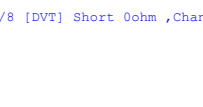
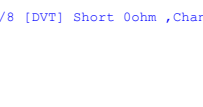
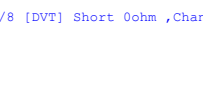
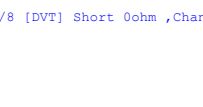
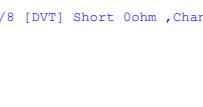
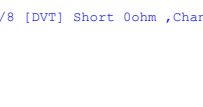
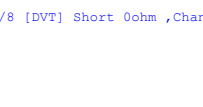
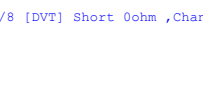
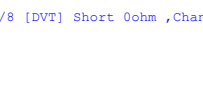
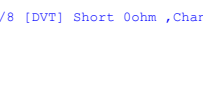
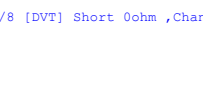
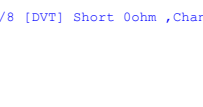
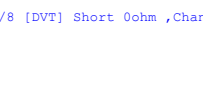
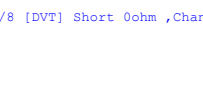
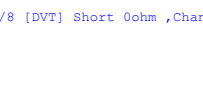
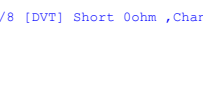
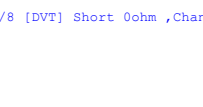
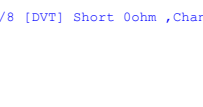
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

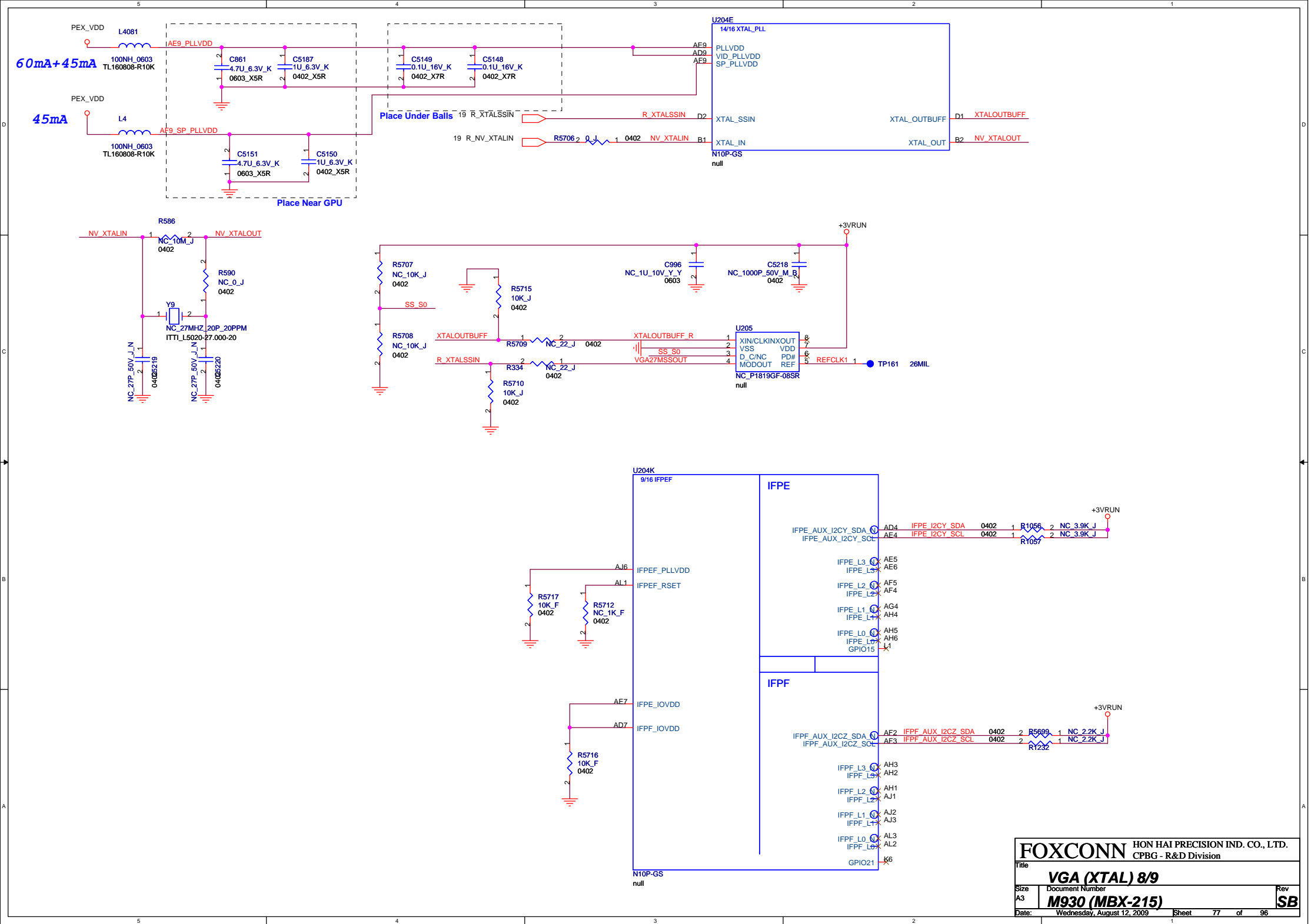


7/8 [DVT] Short 0ohm, Change Net name.

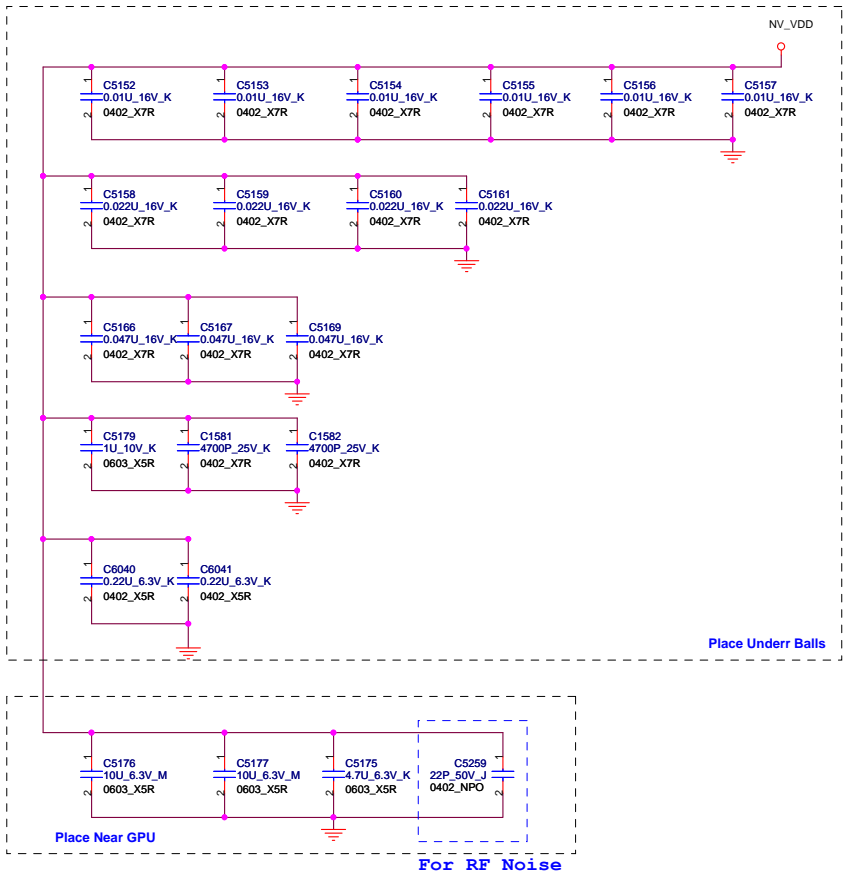
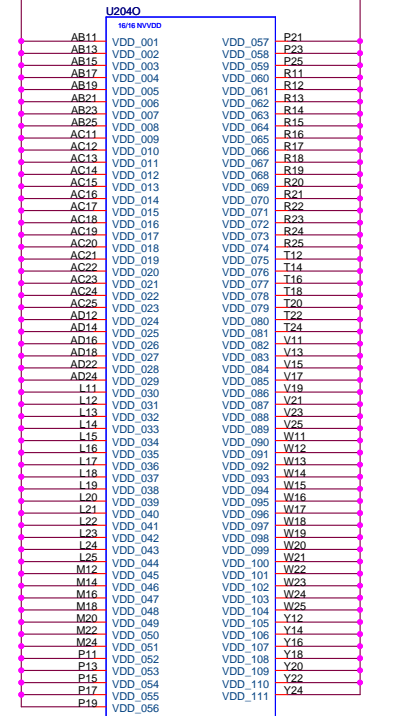


8/4 [DVT] Stuff R5705 as FAE Request.



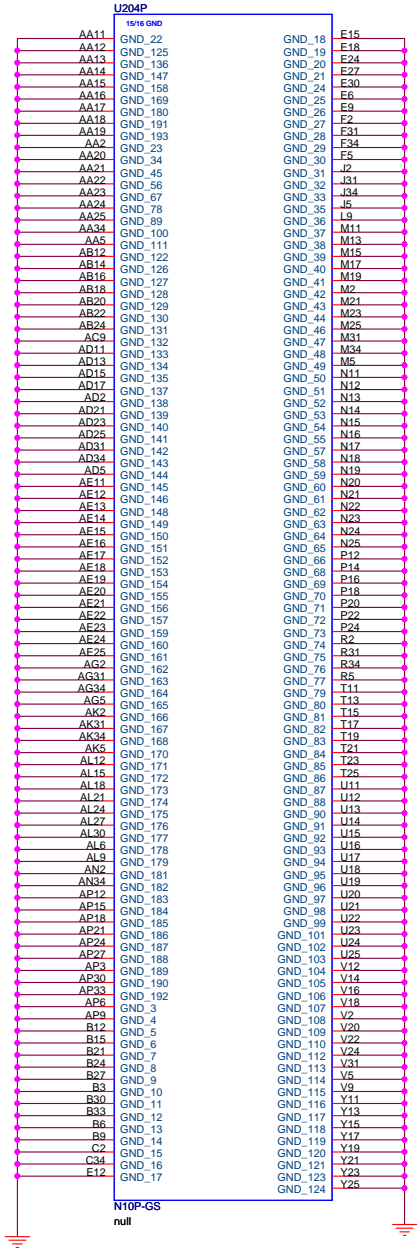


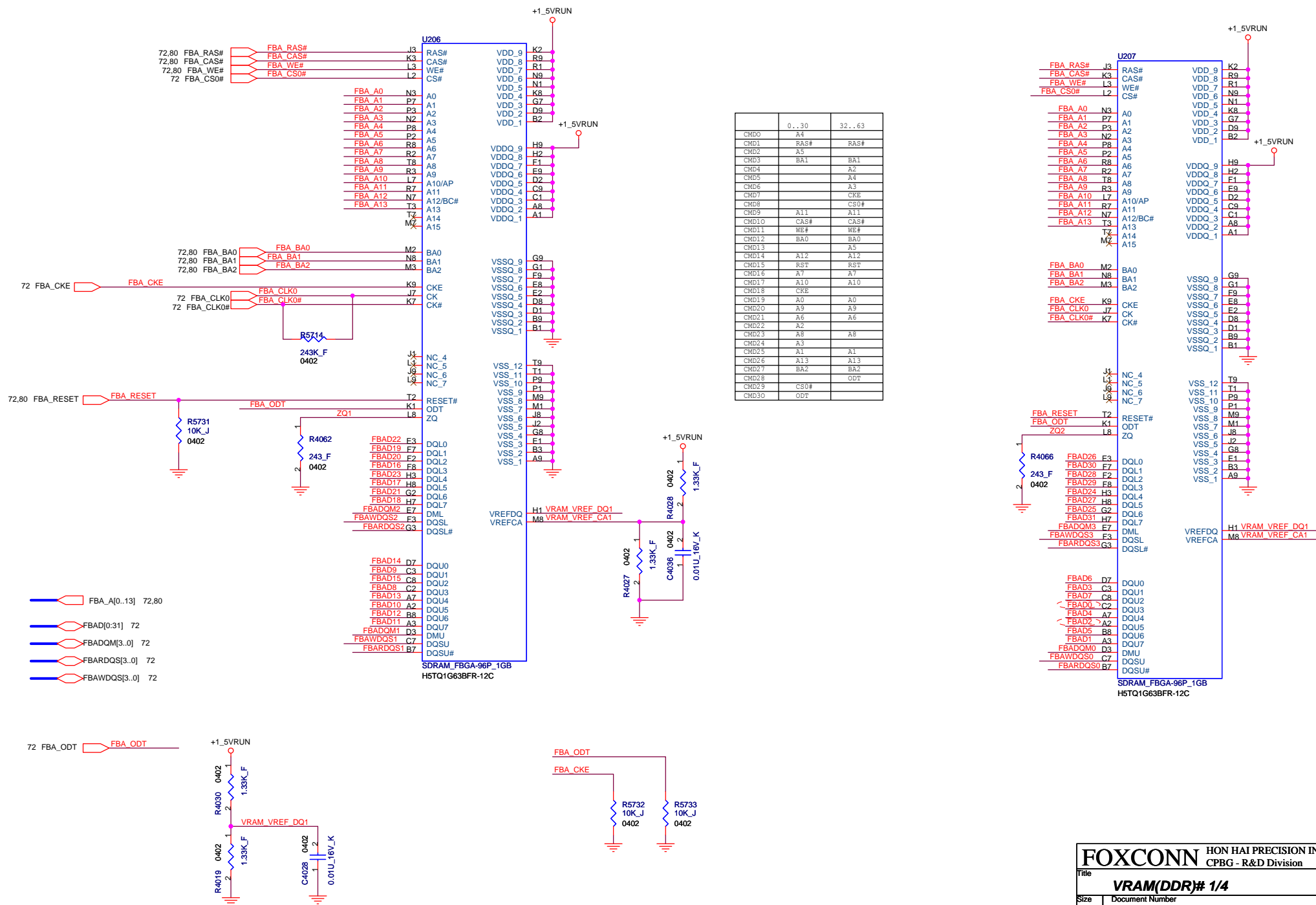
31.66A (N11P-GE1)
16.77A (N11M-GE1)

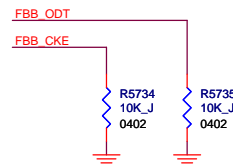
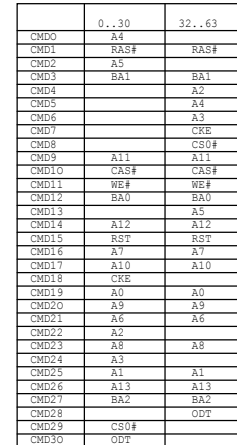


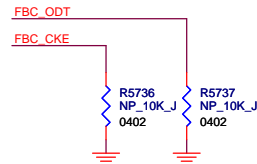
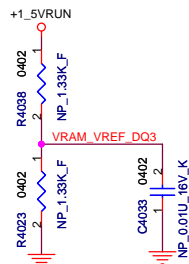
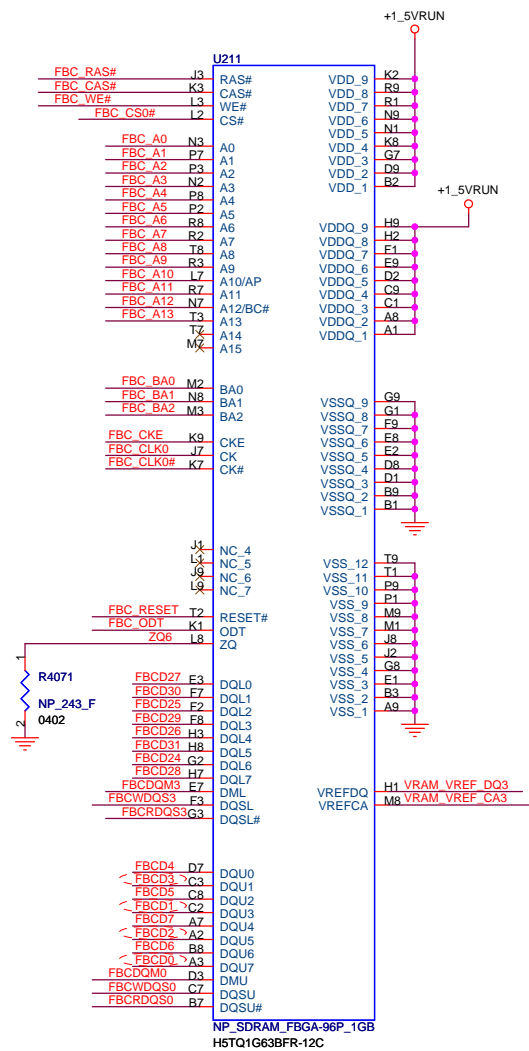
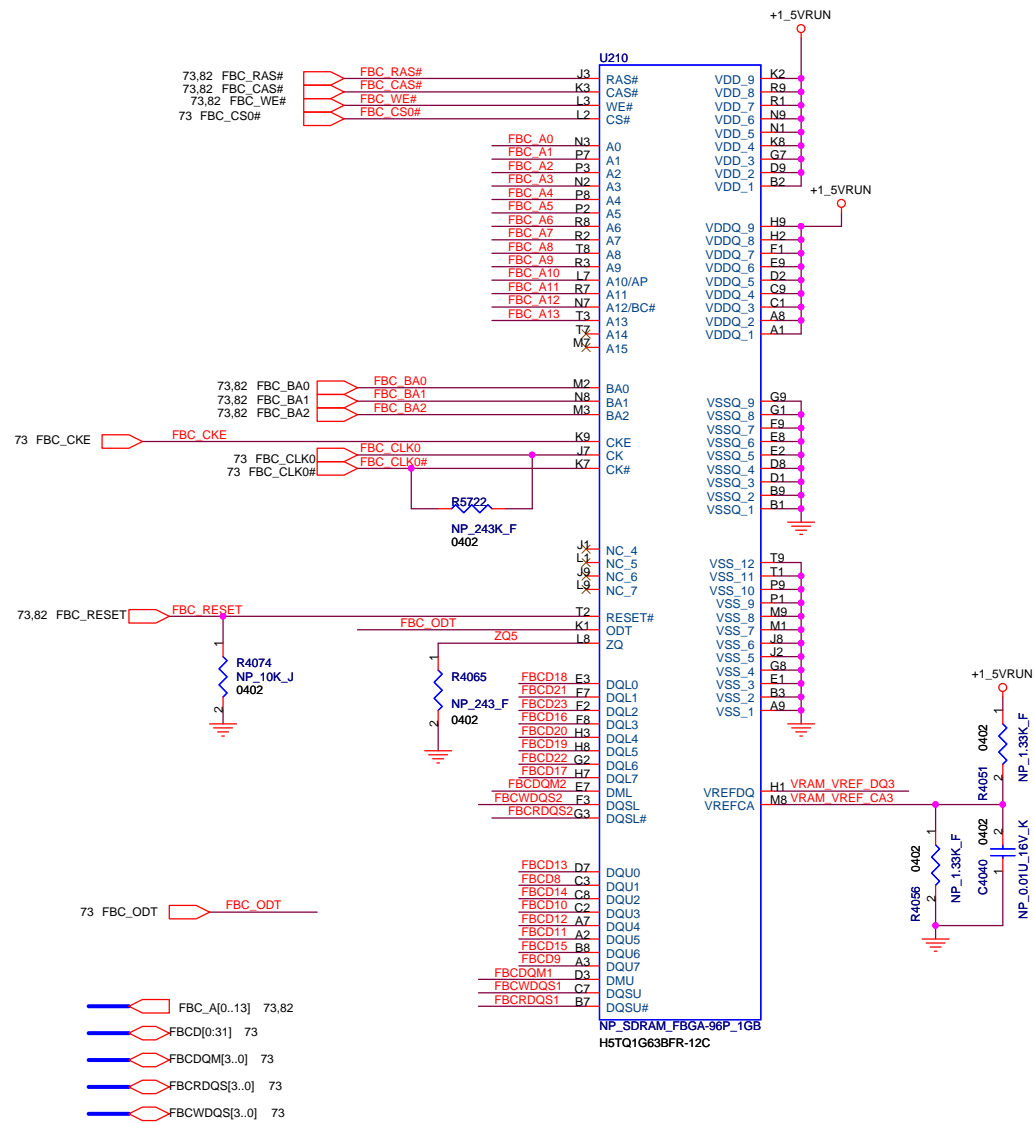
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

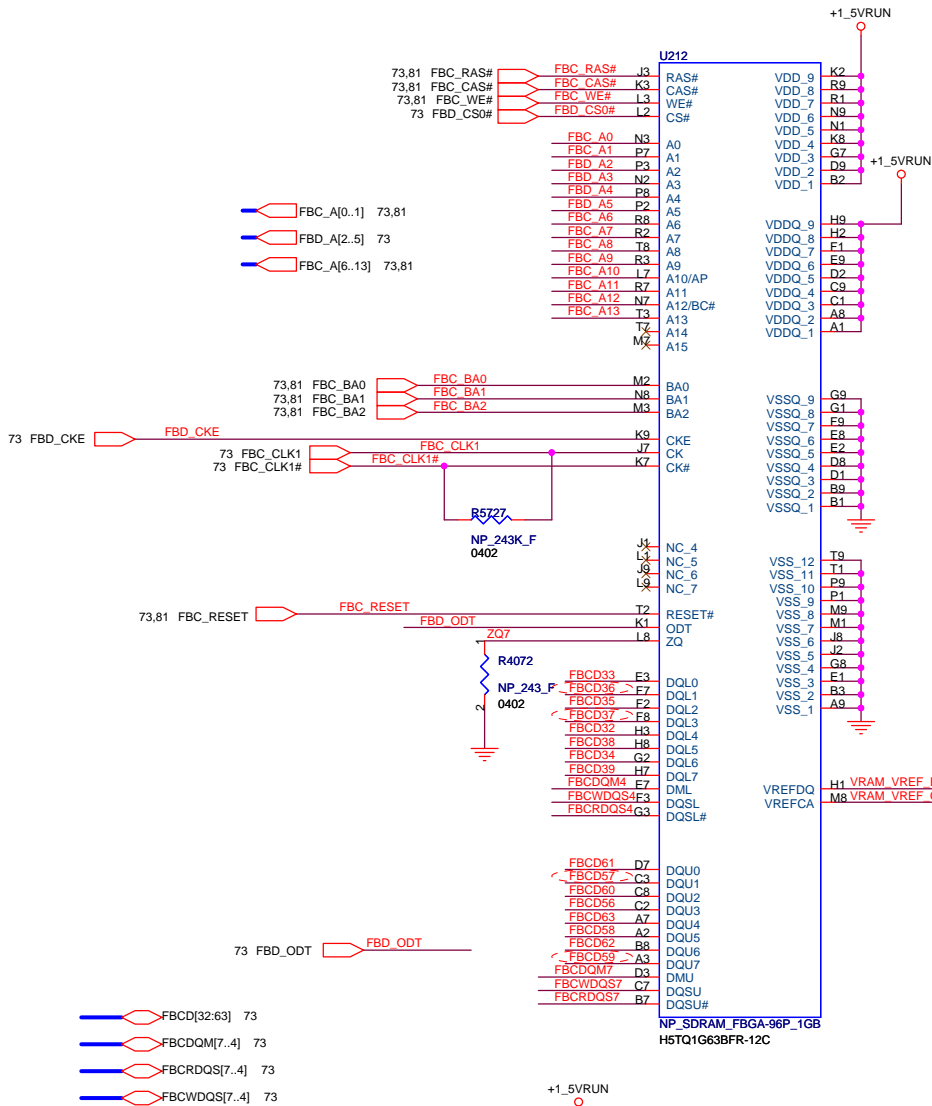
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



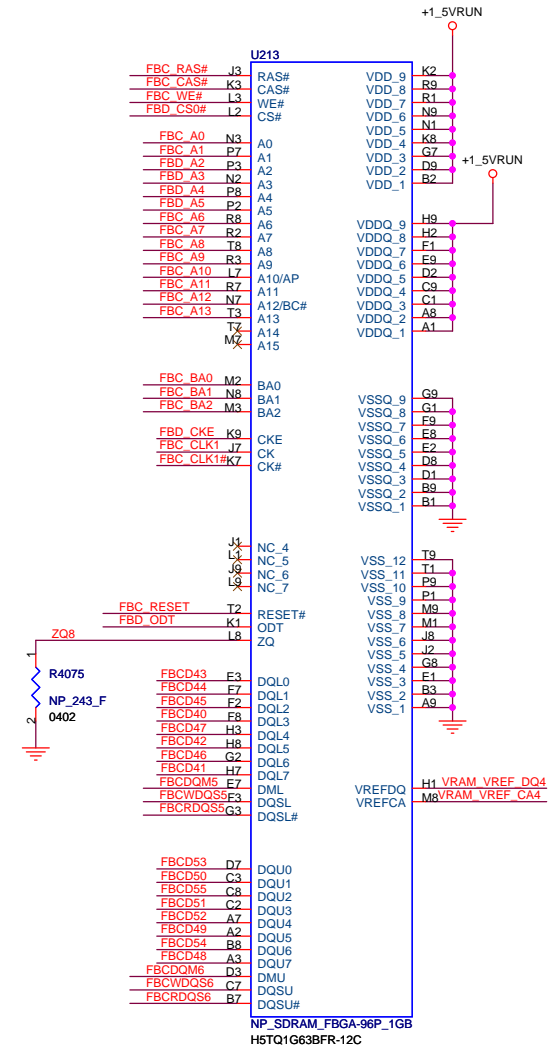




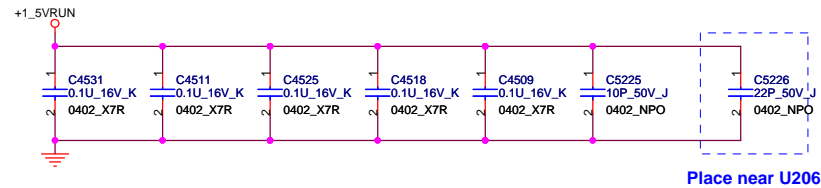




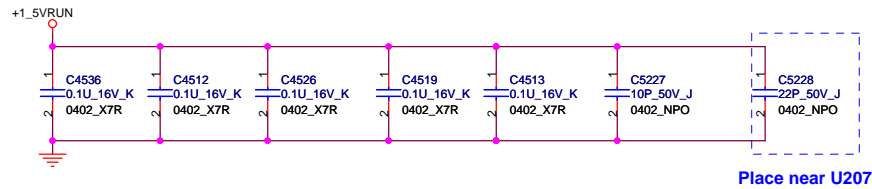
	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	A7	CSE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	



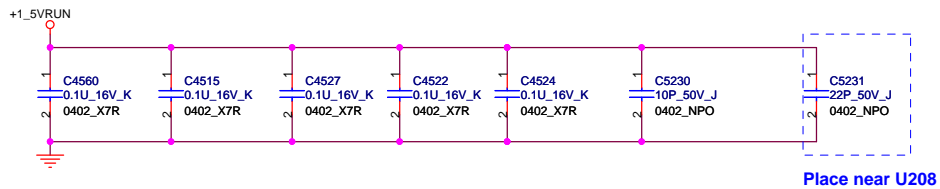
Place around the VRAM U206



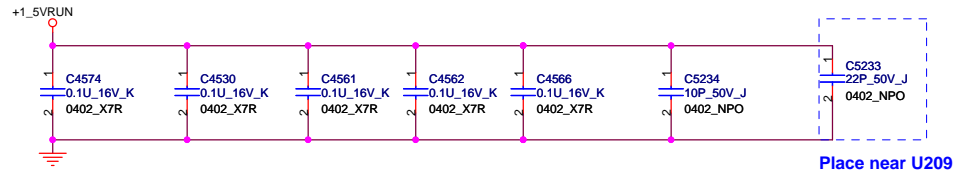
Place around the VRAM U207



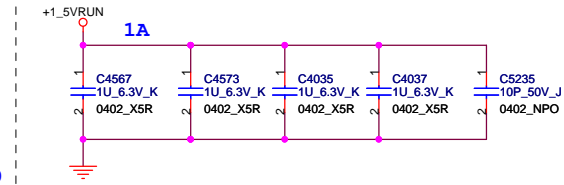
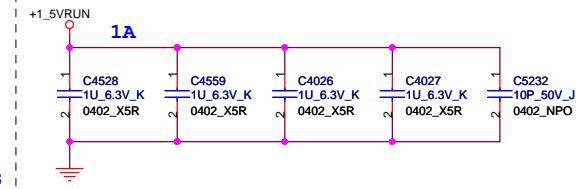
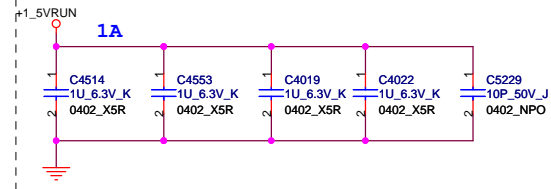
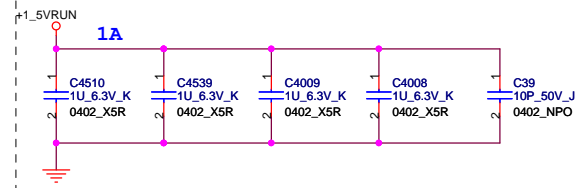
Place around the VRAM U208



Place around the VRAM U209

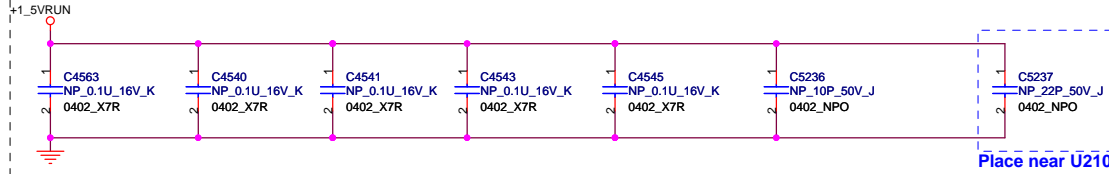


PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

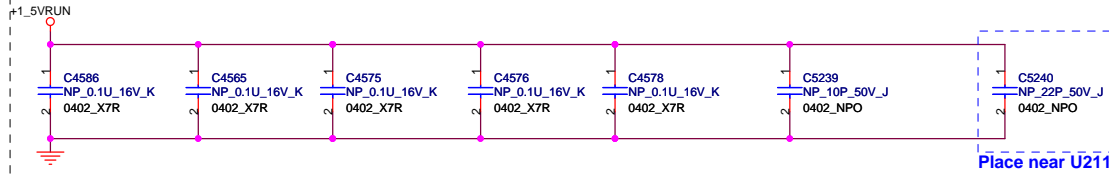


PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

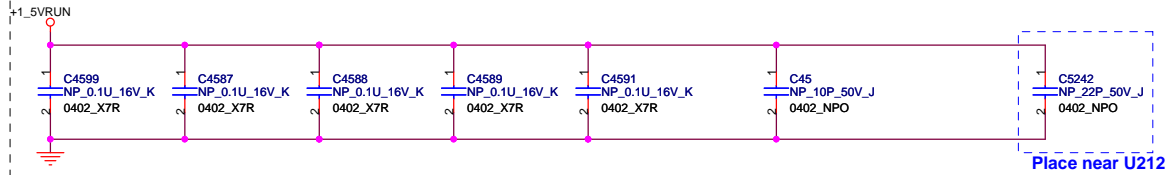
Place around the VRAM U210



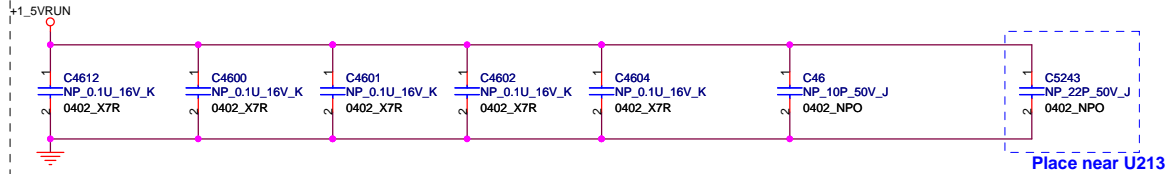
Place around the VRAM U211



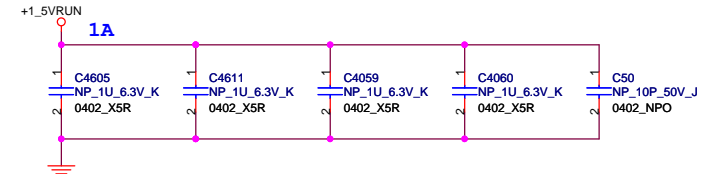
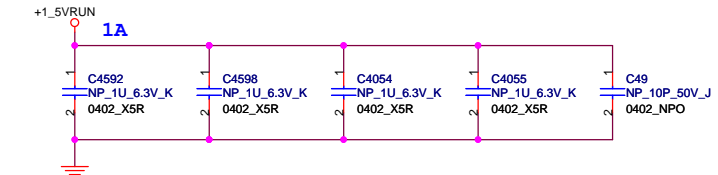
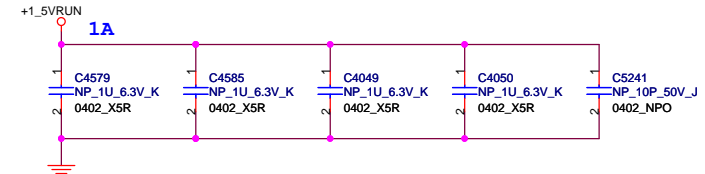
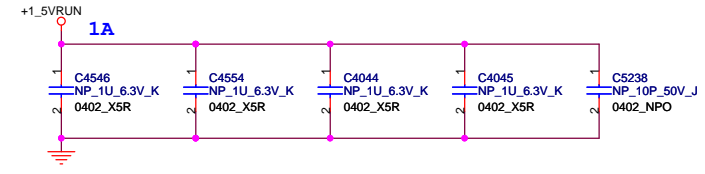
Place around the VRAM U212



Place around the VRAM U213



PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.



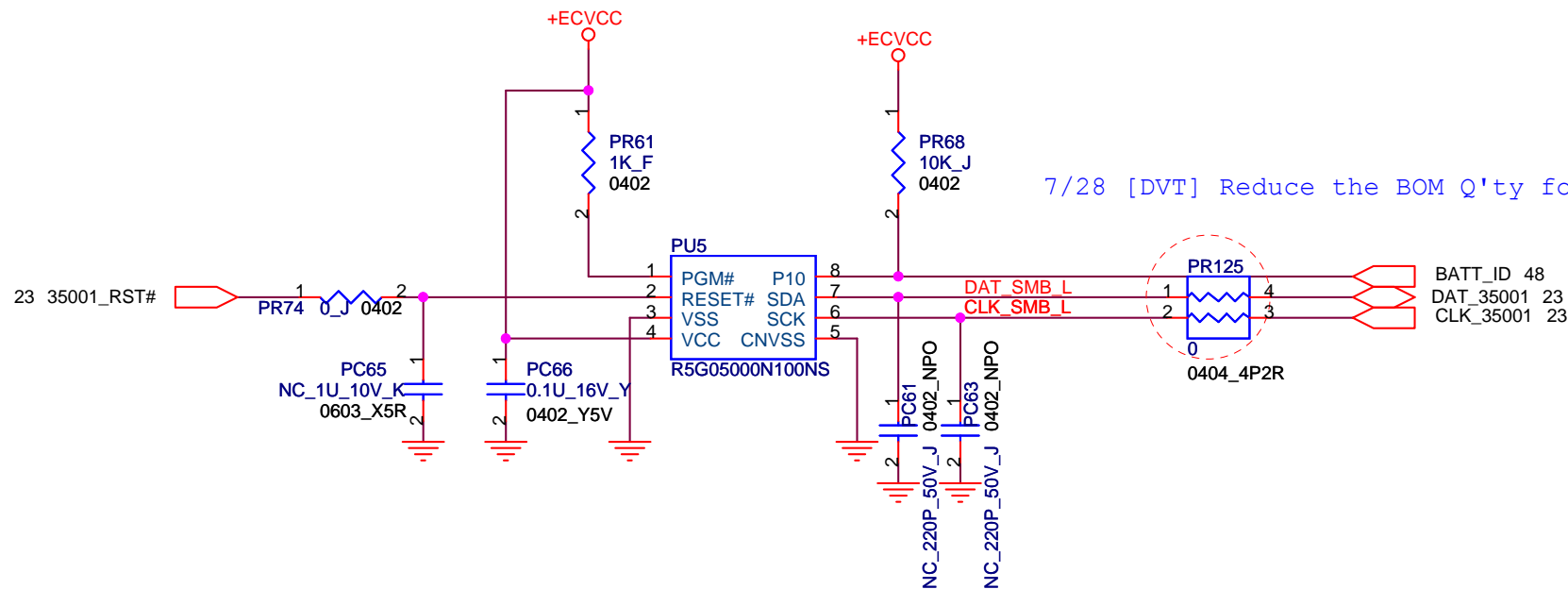
PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.



Co-lay



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <i>LID SWITCH & USB/eSATA Combo</i>			
Size C	Document Number <i>M930 (MBX-215)</i>	Rev <i>SB</i>	
Date: Wednesday, August 12, 2009		Sheet 85	of 95

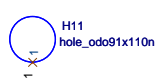
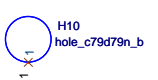
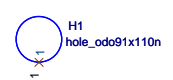
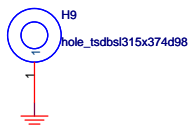
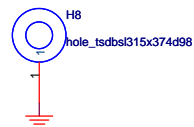
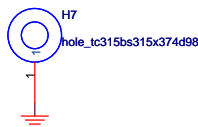
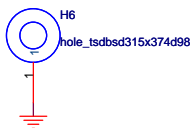
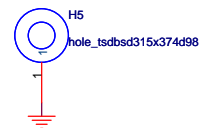
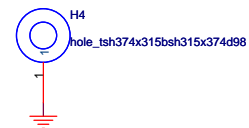
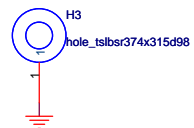
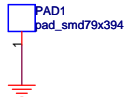
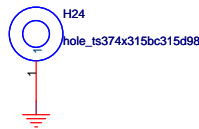


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <i>Identify IC</i>			
Size A	Document Number <i>M930 (MBX-215)</i>		Rev <i>SB</i>
Date:	Wednesday, August 12, 2009	Sheet 86 of 96	

AMI Label (For MP Only)

TABLE1
NC_AMI-APTIO

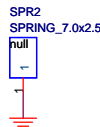
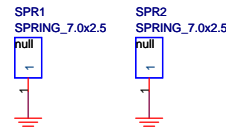
MB PAD & Screw Hole



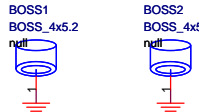
NPTH

7/13 [DVT] Change BOSS3/BOSS4 P/N.

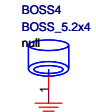
7/9 [DVT] Revise BOSS5 Footprint Symbol



EMI SPRING



WLAN Module



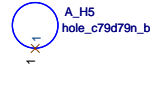
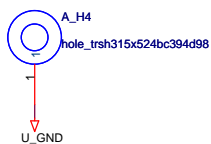
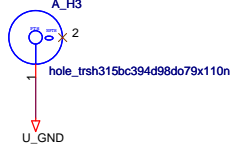
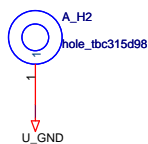
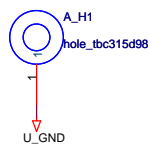
Thermal Modul



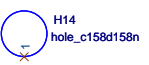
Bluetooth Bracket



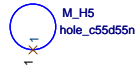
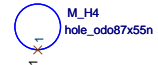
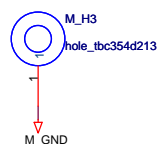
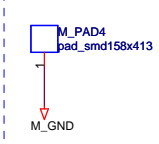
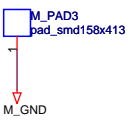
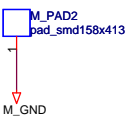
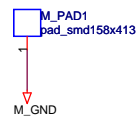
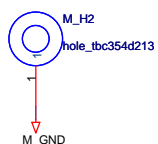
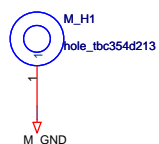
T-jet (MACH)



Audio & USB DB



CPU Plate

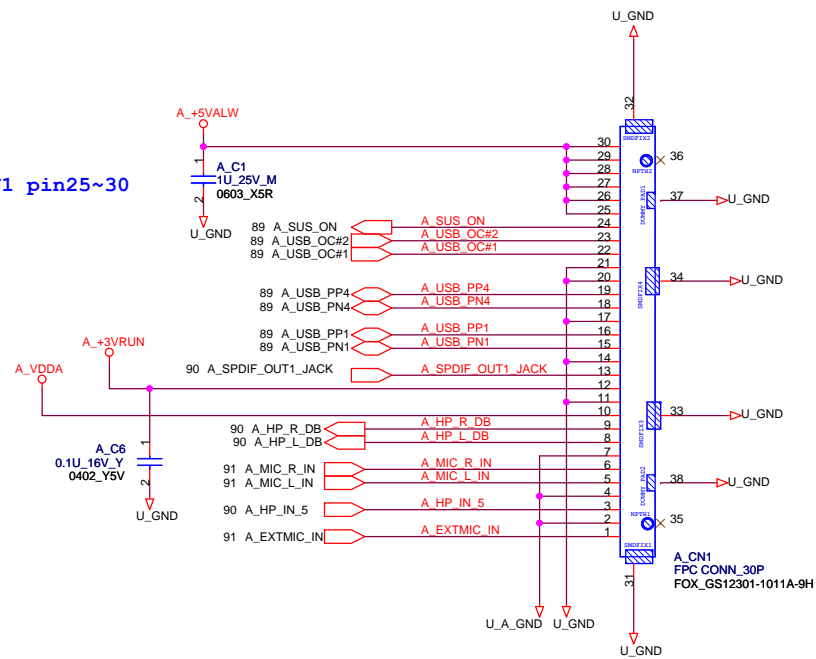


Switch DB

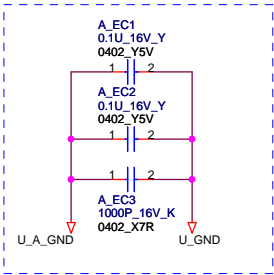
7/16 [DVT] Add M_PAD4 as ME request

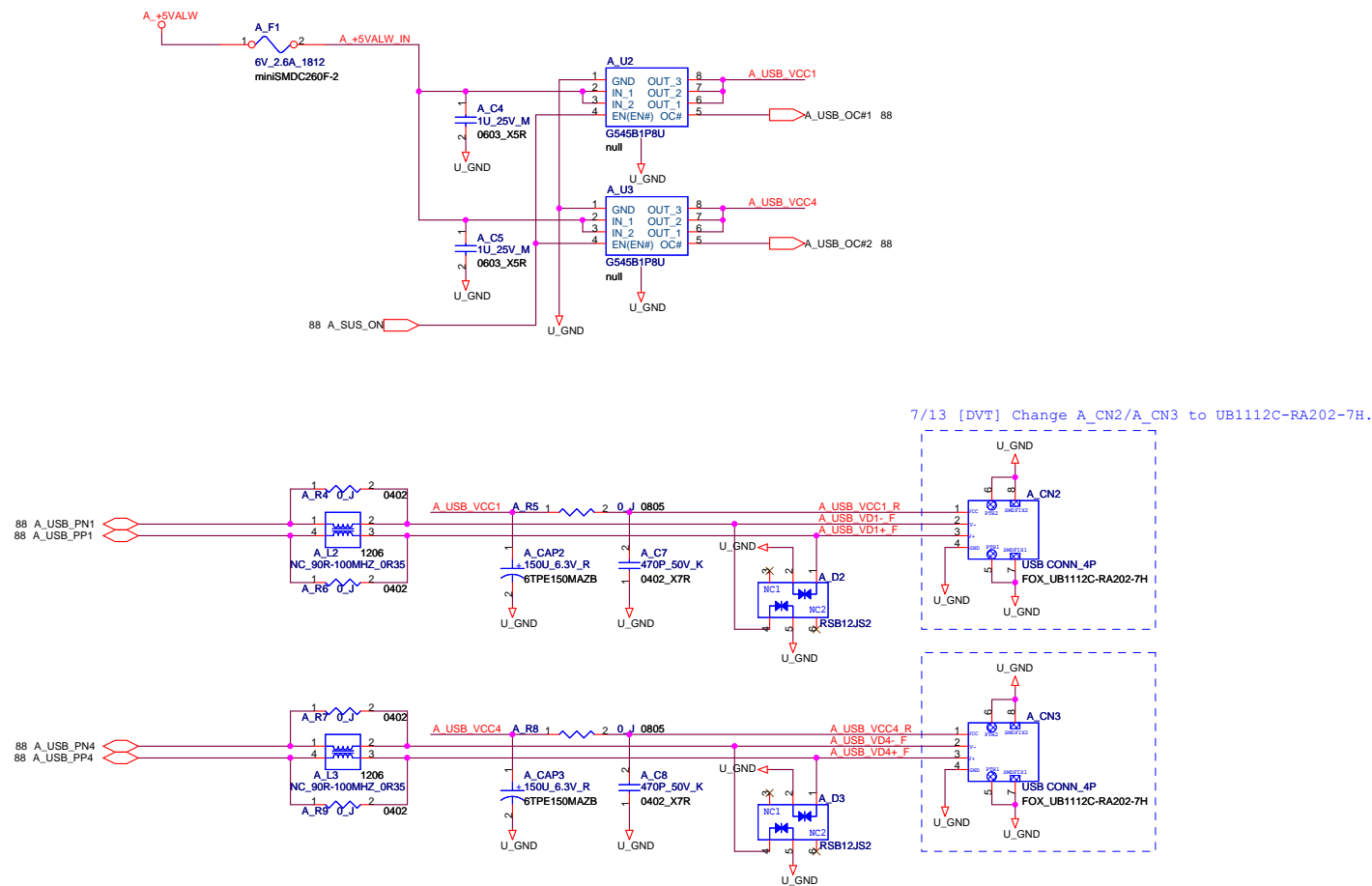
7/16 [DVT] Revise M_H3 as ME design change.

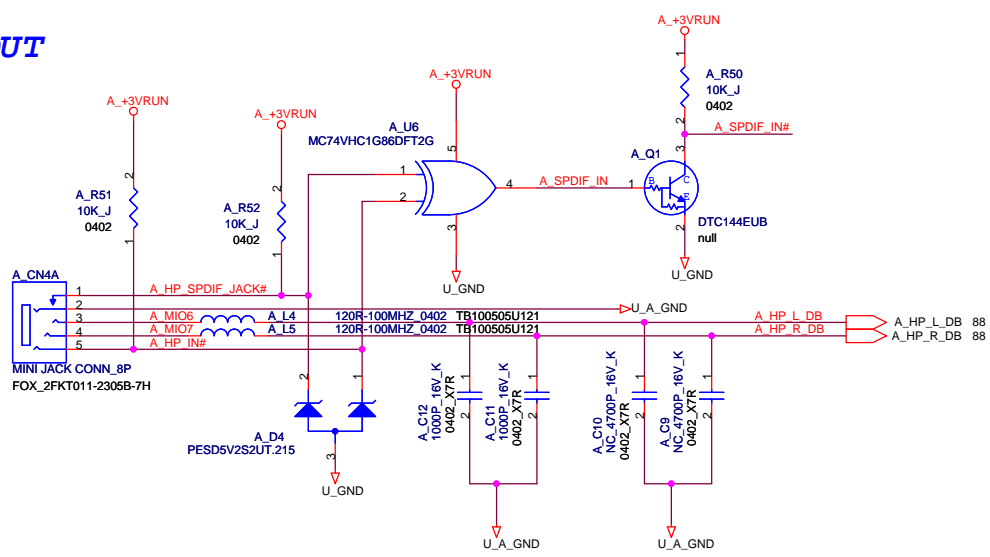
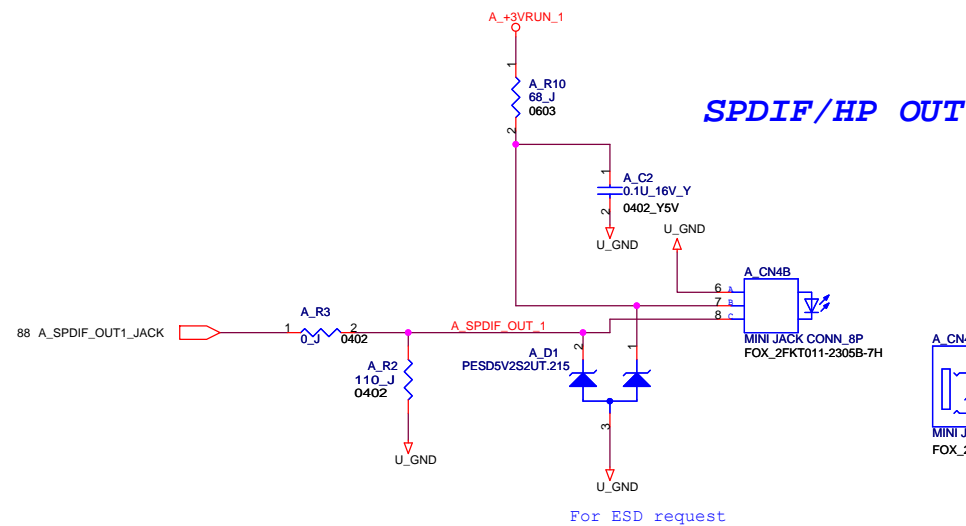
Place A_C1 close to A_CN1 pin25~30



8/5 [DVT] Add EMI Solution A_EC1~3.

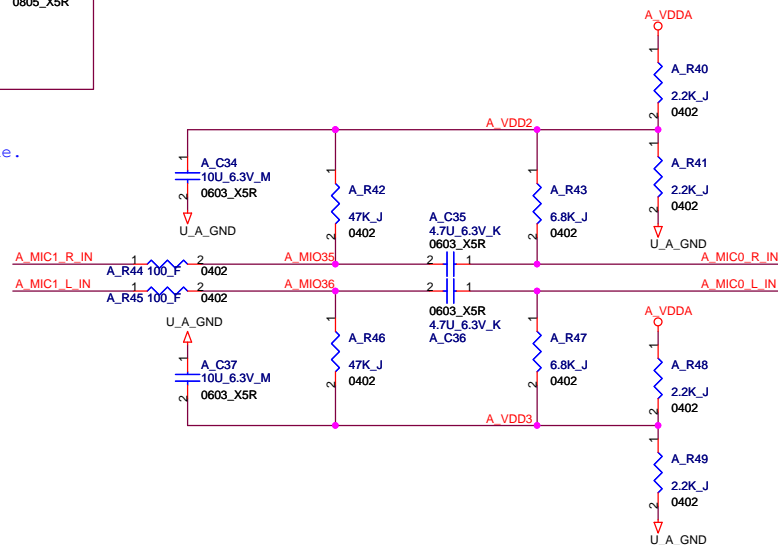


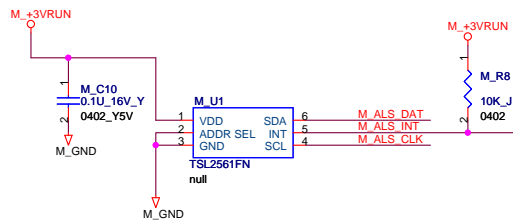




LED status

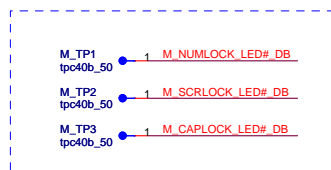
	Pin 1	Pin 5	A_SPDIF_IN#	A_HP_IN_5
HP	0	0	1 off	1
SPDIF	0	1	0 on	0
No plug	1	1	1 off	0



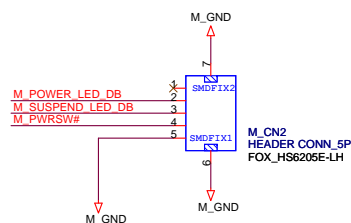


Ambinet Light Sensor (TAOS)

Slave Addr: 52h(W) , 53h(R)
(Pin2 ,Addr Select :GND)



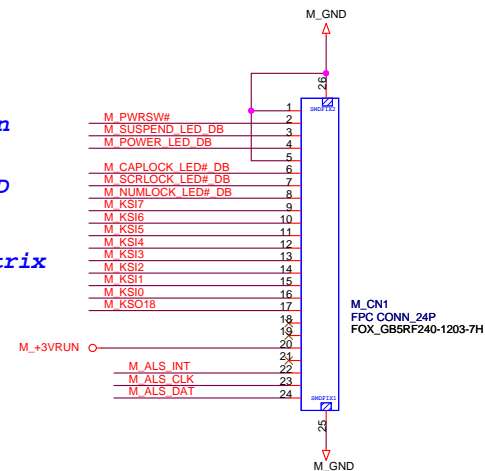
8/12 [DVT] Add Test Point for L6 Test JIG.



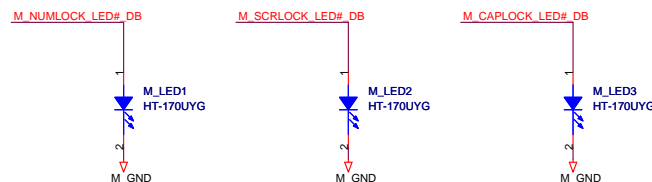
Power Button Conn

Power Button
Keyboard LED
Switch Keyboard Matrix

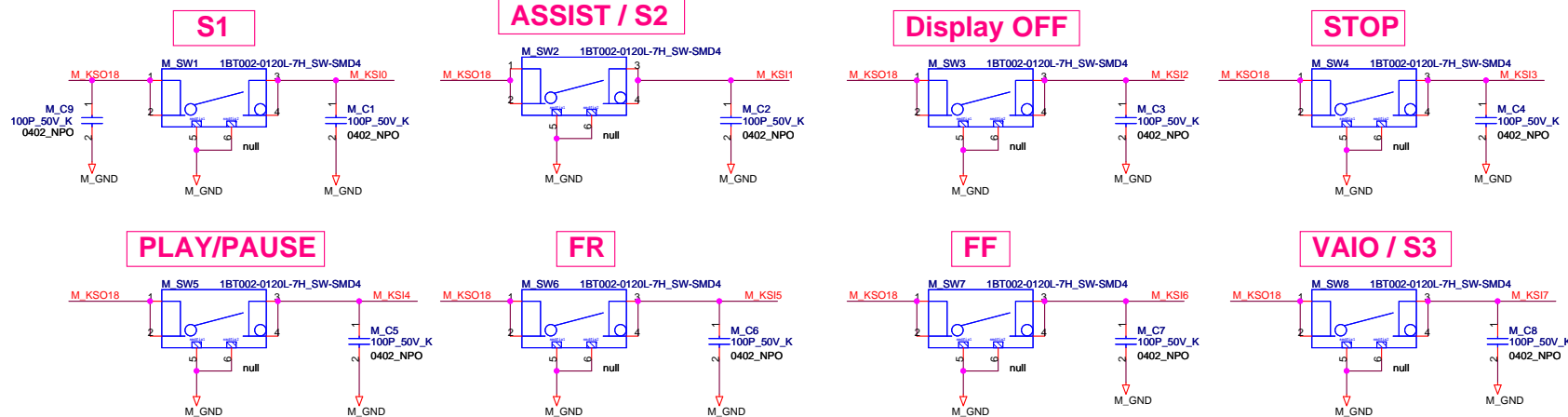
Light Sensor



Switch DB Conn



Keyboard LED



(2009/04/21)

P.87 {HOLE} Add Audio&USB DB PAD
P.11 {PCH} Add R5421 PH 10Kohm to +3VALW
P.90 {SPDIF} Revise LED Status Table

(2009/04/22)

P.71 {VGA Strap} ROM_SI Table Revised
P.71 {VGA Strap} Revise R5219 value to NVH_
Revise R5199 value to NVS_
P.01 {Index} Revise M930 BOM Control Table
P.34 {PCIE(SD)} Add R820/R817 and C868/C865 for VEDS_I/F_Memory Card
P.34 {PCIE(SD)} Revise net name from SD_WP to SD_WP#
P.87 {HOLE} Add CPU Plate NPTH Hole, H12, H13 ,H14 ,H15
P.01 {Index} Add MB PCB P/N
P.41 {Backlit Conn} Revise PWM by +5VRUN
P.41 {Backlit Conn} Revise CN39 Pin2 as KB_PRESENCE
P.41 {Backlit Conn} Revise R695 from 150ohm to 0ohm

(2009/04/23)

P.91 {Ext MIC} Change A_C35,A_C36 to 4.7uF/X5R
P.10 {PCH} Change R158 from Stuff to Dummy
P.10 {PCH} Change R156 from 1Kohm to 0ohm
P.51 {VTT POWER} Change design the PQ66 logic for MOR request
(low enable voltage concern)
P.09 {MCP} Change R1272 to Dummy_3.01Kohm
P.20 {DIMM} Add CAP13 330uF for +1 5VSUS
Change CAP12 100uF to 330uF

(2009/04/24)

P.29 {LAN} Change GbE Solution to 88E8059 (7x7mm)
P.23 {EC} Add Test Point , TP185, TP277 ,TP287

(2009/04/27)

P.34 {PCIE(MS)} Add R1467 damping resistor for MS_CLK as FAE suggestion
P.34 {PCIE(MS)} Dummy R76 of SDMSXD_VCC as FAE suggestion
P.34 {PCIE(MS)} Change C540 from 1uF to 10uF as FAE suggestion
P.28 {TV} Revised PC84 location to C85
P.53 {SYS Power} Revised U85 location to PU18
P.74 {Graphic} Add Net Name for U204 ,Pin AC6 ,AK8
P.75 {Graphic} Add Net Name for U204 ,Pin AK9, AG9 ,AJ9 ,AJ8
P.77 {Graphic} Add Net Name for U204 ,Pin AE9 ,AF9
P.37 {Felica} Add Current Limit IC (U48) for MOR request.
P.67 {Audio AMP} Revise the R360 and R363 from 47Kohm to 1Kohm.
P.68 {Audio AMP} Revise the R1,R2 ,R3 ,R4 from 3.3Kohm to 8.2Kohm as MOR revised.
P.68 {Audio AMP} Add the P_GND for AMP to isolate the AMP GND plane.
P.28 {TV} Update Saturn information from MOR. Change Pin definition as Doraemon.
P.43 {Touch Pad} CN6 Swap Pin Definition for ME design review w/FFC.
P.41 {Backlit KB} CN39 Swap Pin Definition for ME design review w/FFC.
P.30 {Transformer} Delete C811 and C812 ,Change C809 GND_TR to GND.
P.85 {USB/eSATA} Add D15 and D16, D24 for signals ESD protection.
P.23 {EC} Add C418/C513 (47P) for GPIOs Expander SMBus.
P.92 {Switch DB} Add M_SW9 for ASSIST.
P.23 {EC} Change R63/R64 from 100ohm to 0ohm.
P.34 {PCIE(MS/SD)} Add 0ohm damping on the MS/SD bus and close to U71.
P.51 {VTT POWER} Revise the resistor divider value of PR505 and PR506.

P.34 {PCIE(MS/SD)} Revise the MS/SD Power Netname as MS_VDD and SD_VCC.
P.19 {CLK GEN} Delete RP86 and use 2 resistors(R584/R595)for NV_27MHz.
P.62 {HDMI} Delete RP46
P.74 {Graphic} Dummy R5694/R1229, there are the PH on Page63 already.
P.63 {CRT} Leave NC for Semi-PNP Circuit.
P.72 {Graphic} Leave NC R5560.
P.73 {Graphic} Leave NC R5561.
P.77 {Graphic} Delete R5711
P.11 {PCH} R1593 and R1594 revise to 2.2Kohm.
P.16 {PCH Power} R823 change from 0603 to 1206 for VCCIO(3A).
P.43 {Touch Pad} Change F9 to 1M-F10V0A1-F000 as MOR request (0.12A)
P.43 {Touch Pad} Reserve the +3VRUN Power Source path for Synaptics.
P.76 {Graphic} Stuff R1105 and R1106 for U204, I2C Bus.
P.45 {FAN} Revise the Direct PWM circuit. (Refer to M860)
P.74 {Graphic} As FAE suggestion, revised eDP to IFPD port.
P.77 {Graphic} As FAE suggestion, revised HDMI to IFPE port.

(2009/04/28)

P.23 {EC} Add U25 GPIOs expander and revised the GPIOs pin assignment.
P.92 {Switch DB} Add M_SW9 ,and Change the M_CN1 Pin Assignment (KS018/KS019).
P.40 {Switch Conn.} Change the CN2 Pin Assignment (KS018/KS019).

(2009/04/29)

P.35 {SD} Change the C518/C522 from Y5V to X5R.
P.28 {TV} Add the C88 and C94 for +3VRUN_CN16 ,Add C87 for +1_5VRUN_CN16 as MOR request.
P.27 {WLAN} Delete C-Link Bus as MOR request.
P.27 {WLAN} Dummy R17, Pin #24 is defined as NC on PumaPeak/KilmerPeak/Atheros modules. (MOR side comment)
P.27 {WLAN} Stuff R1560 and Remove R1557 then short to GND.
P.27 {WLAN} Leave NC U45 and C891 then add RP12 Jumper.
P.27 {WLAN} Change D1 to BD4148FPT.
P.27 {WLAN} Change Q5 to from FET to BJT(DTC144EUA).
P.61 {LVDS} Add C97 for U46 Power supply.
P.39 {BT} Change BT connector CN22 to FOX_QT510106-312H-7H.
P.4 {MCP} Change R262 from 2.2Kohm to 4.7Kohm as MOR request.
P.62 {HDMI} Change R504 from 2.2Kohm to 4.7Kohm as MOR request.
P.77 {Graphic} Add PH resistor R5699 and R1232 Bus Mater of IFPF.
P.72 {Graphic} Delete J27 pin circuit and leave NC.
P.77 {Graphic} Add Bead/Caps for IFPE Power (+3VRUN/PEX_VDD) (HDMI).
P.76 {Graphic} Leave NC R1779 as FAE suggestion.
P.71 {Graphic} R577 for Strap1 revise to 35Kohm setting (0110) as FAE PUN revised. (PUN-04335-001_v08.pdf)
P.76 {Graphic} Delete R5252 as FAE Suggestion.
P.57 {NV_VDD} Swap PWRCNTL_0 and PWRCNTL_1 Signal.
P.48 {DCIN&CHARGER} PR12 change from 51K to 59Kohm for 90W DPPM(4.2A)Revised.
P.68 {SPK} Change Bead to 0ohm for FAE Suggestion.
P.61 {LVDS} Revise PANEL_ID Table by SW Requirement.
P.70 {Graphic} Revised the U204, Pin AG19,Pin F7 from NV_VDD33 to +3VRUN as FAE suggestion.

(2009/04/30)

P.28 {TV} Add CN16, Pin1/Pin2 from EC control CIR module (Reset#/Wake#).
P.23 {EC} Add CIR Control Signal(RST# and Wake#) and Swap GPIOs Pins.
P.65 {AUDIO} Add comment when implement ALC275.
P.67 {AUDIO} Add comment when implement ALC275.
P.68 {AUDIO} Add comment when implement ALC275.

(2009/05/01)

P.11 {PCH} Revise the R566/R5420 PH Power plane to +3VSUS.

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(2009/05/04)

- P.59 {OVP} Stuff PR88 and Change PC41 to 1000pF as MOR suggestion.
P.12 {PCH} Add the R927 for the MEPWROK Path (RUN PWRGD) and Dummy R918.
393353_393353_Calpella_Power_Seq_Spec_Rev1.1 requirement.
P.87 {HOLE} Add the HOLE P/N for Switch DB.

(2009/05/05)

- P.76 {Graphic} Add R2319/R2320 10Kohm PD for GPIO5 ,GPIO6.
P.All {All} Review Test Point for the BFT/Power Test and Debug usage.

(2009/05/06)

- P.59 {OVP} Add PQ10 for EC Control to reduce SKU. (EVT evaluation usage)
P.48 {DCIN&CHARGER} Add PQ7 for EC Control to reduce SKU. (EVT evaluation usage)
P.23 {EC} Add R71 PD for EC_PWRLIMIT_CTRL. (U4, Pin113)
P.61 {LVDS} Add J2 and J3 for DIS_FAN_MON#. (BFT Test Usage)

(2009/05/07) - Pre-BOM 0.70

- P.35 {MS/SD} Change the LED4 from Side View to Front View as ME request.
P.63 {CRT} Add R5752 for VGA_CRT_DET# for MOR Request.
P.62 {HDMI} Change R515 and R538 from 2.2Kohm to 3.9Kohm for MOR Request.
P.63 {CRT} Change R471 and R472 from 2.2Kohm to 3.9Kohm for MOR Request.
P.76 {GRAPHIC} Leave NC for R2317.
P.60 {INV Conn} Change R405 from 100Kohm to 10Kohm.
P.41 {KB} Revise the Net name from KB_PRESENCE to KB_PRESENCE#.
P.23 {EC} Revise the Net name from KB_PRESENCE to KB_PRESENCE#.
P.23 {EC} Reserve the RP23 for +3VRUN Path for Touch Pad.

(2009/05/08)

- P.87 {HOLE} Revise the H1 as MERD Request
P.92 {Switch DB} Revise the M_CN1 Pin Definition as MERD Connector Design Changed.
P.75 {GRAPHIC} Leave NC for R1056,R1057.
P.75 {GRAPHIC} Leave NC for R5699,R1232.

(2009/05/11)

- P.85 {USB/eSATA Combo} Add CN27A Pin1 Net Name as USB_VCC0_R.
P.48 {DCIN&CHARGER} PCN1 Connector Pin8 and Pin9 Change NPTH to PTH Grounding usage.
P.39 {BT} Add U1,R6,C6 for BT Module leakage protection.
P.23 {SODIMM VREF} Delete M2 Path as Intel Update
P.9 {MCP} Leave RP83 as NC as MOR Suggestion.
P.4 {MCP} Revised the COMP Signals Layout Notices
P.28 {TV} Change F12 from 1.5A to 2A (1812L200-C) as MOR Suggestion.
P.38 {LVDS/eDP} Add the +3VRUN Power Source for eDP requirement and add the C1364,C1365,C5260
P.10 {PCH} Add R298 the +3VALW Power for GPIO13/ GPI default usage.
P.26 {ExpressCard} L38,L39,L40 Net Swap for Layout Routing Requirement.

(2009/05/12)

- P.87 {HOLE} Add PAD1 as MERD Request
P.38 {LVDS/eDP} Change C1362/C1364 from 0805 to 0603.
P.87 {HOLE} Revise the H4 as MERD Request.
P.23 {EC} Add R55/R41 PH for GPIOs Expander SMBus.
P.23 {EC} Add R57 PH for OVT EC#
P.23 {EC} Add R59 PH for KB_PRESENCE#
P.23 {EC} Add R72 PH for EXT_INT#
P.92 {SW DB} Revise the SW Table Description and Delete M_SW9.
P.35 {SD} Change NET name SD_CLK to SD_CLK_R on C767.

(2009/05/13)

- P.10 {PCH} Change CN26 Symbol of RTC BAT.
P.71 {GRAPHIC} Add N11P/N11M Device ID, 0CAF/0A75.
P.23 {EC} Delete HARD_RST#/CIR_WAKE# and Swap GPIOs
P.85 {USB/eSATA Combo} Add U214 SATA Reapter for Total Length Issue.
P.23 {EC} Add EC_IADAPT for Power Current Monitor (Reserve for EVT evaluation)
P.48 {DCIN&CHARGER} Add PR34 for EC Power Current Monitor (Reserve for EVT evaluation)
P.48~57 {Power} Change the Power Jump 1X-JUMP000-0031 as Power RD Request.

(2009/05/14)

- P.87 {HOLE} Add the HOLE P/N H16~H19 for BAT/ODD Connector.
P.87 {HOLE} Add the HOLE P/N H20~H23 for ExpressCard Connector.
P.87 {HOLE} Add the HOLE P/N H24 for MB Screw.

(2009/05/15) -M930 EVT_MB_ALC275_0515-1030

- P.64 {CODEC} Change Solution to ALC275 as MOR Request.
P.90 {S/PDIF} Change A_C9/A_C10 from 1206 to 0402 as Same 0.047u/X7R/0402 (NC).
P.77 {Graphic} As FAE suggestion, Connector U204K,pin AE7 and AD7 as IFPE_IOVDD.
P.75 {Graphic} As FAE suggestion, Connector U204J,pin AJ8 as IFFD_IOVDD (AK8).
Delete L2, C66,C5138,C5137,C5136
P.87 {HOLE} Update A H3, A H4 for USB DB PAD revised as MERD Request.
P.62 {HDMI} Delete R513 and add D25 as FAE suggestion.
P.70 {Graphic} Add C91 for NV_VDD33 as DG_v0.4.
P.63 {CRT} Change F2 to 6V-0.35A 1206 for MOR Request.
P.71 {GRAPHIC} Review the Strap Table for N10x/N11x support.

(2009/05/16)

- P.48 {DCIN&CHARGER} Change PF1 to 32V-7A 1206 as PUR Suggestion.
P.10 {PCH} Delete R302 and Change R1553 to 150ohm.
P.17 {PCH} Add R1617 PH Resistor (NC).
P.10 {PCH} Add R1557 for +3VRUN Jump and D23 Leave NC on EVT evalution.
P.48 {DCIN&CHARGER} Add PR45,PR46 for EC_VADAPT for EC Power Monitor. (Reserve for EVT evaluation)
P.23 {EC} Add C6072 for EC_VADAPT Signal.
P.68 {SPK} Revise the Comment for the Cable Short circuit.
P.9 {MCP} Add NET Name for RP83, DQ_VREF0_J17 and DQ_VREF1_H17.

(2009/05/18)

- P.64 {CODEC} Add R5794/R5795 for P_GND Isolation as MOR Request.
P.75 {GRAPHIC} Change the HDMI port to C as FAE Revised.
P.77 {GRAPHIC} Change the HDMI port to C and Disbale the Port E.
P.64 {CODEC} Add Q90 for Switch +5VAMP (PVDD1/PVVD2 Power Down) as MOR Request.

(2009/05/19)

- P.64 {CODEC} Revise the Thermal PAD to P_GND Isolation as MOR Request.
P.64 {CODEC} Add some comment for Placement as MOR Request.
P.64 {CODEC} Change C6056/C6057/C6061/C6062 as DGND to P_GND as MOR/FAE Request.
P.64 {CODEC} Add Q90 for PVDD1/PVDD2 Power Switch when Cbale Short as MOR Request.
P.64 {CODEC} Add C368 for S/PDIF EMI concern as FAE Suggestion.
P.64 {CODEC} Add C6073 for DVDD as MOR Request.
P.65 {MUTE} Revise Q15,Pin3 as AMP_PD# from MOR Request.
P.62 {HDMI} Delete RP55/RP57/RP59/RP61 and RP72/RP73/RP74/RP75 to reduce VIAs and add the common mode filter for dGPU as MOR Request.
P.75 {Graphic} Change IFPC port as HDMI as FAE revised.

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(2009/05/20)

P.64 {CODEC} Change U215 HW_POP_MUTE_CODEC to Pin28 (GPIO2) as MOR Request.
P.69 {TSUB/MACH} Add Q22 for the Module Leakage Concern as MOR Request. (Revised)
P.62 {HDMI} Delete RP53 to avoid the Stub as MOR suggestion.
P.45 {FAN} Reserve the R404 PH resistor.

(2009/05/21)

P.All {All} Change/Review All the Connector to Halogen Free.
P.95 {NV_VDD} Change the PU29 Solution to TPS51217DSCR.
P.51 {PCH Power} Change the PU26 Solution to TPS51218DSCR.
P.23 {EC} Revise the Model_ID Table.
P.23 {EC} Set Model ID to N11x Default.
P.71 {Graphic Strap} Set Strap2 to N11x Default. (Need to Change R value when used N10x.

(2009/05/22)

P.29 {LAN} Change the GbE Solution to Co-Lay 88E8057 and 88E8059 (7mmx7mm)
P.35 {SD} Change the SD LED4 Part.
P.42 {Status LED} Change the LED1, LED2 ,LED3 Part.

(2009/05/23)

P.60 {INV} Change R400 to 10Kohm and Stuff.
P.76 {VGA} Change R2318 to Dummy.

(2009/05/23)

P.90 {HP} Change A_C11 and A_C12 from 0.015uF to 1000pF as MOR suggestion.
P.90 {HP} Change A_C9 and A_C10 from 0.047uF to 4700pF as MOR suggestion.

(2009/05/27)

P.71 {VGA} Revised the N11P/M Device ID for ES Sample ONLY .
N11P-GS1 (ES) : 0A3D
N11M-GE1 (ES) : 0A7D

(2009/06/04)

P.34 {MS} BOM Change R76 as Mount and C540 change to 1uF (1C-2B30105-K002).
P.71 {VGA} Revised the N11P/M Device ID for ES Sample ONLY .
N11P-GS1 (ES) : 0CAD
Revised the N10x/N11x 3GPIO as 1110.

(2009/06/24)

P.23 (EC)Add 0.01uF C6078 for EC_IADAPT.
P.23 (EC)Add R47/10Kohm for MB_FLASH_EN.
P.41 (Backlit)EC Engineer Request, for Backlit conctrol well (+5VALW).
P.19 (CLK)U31 Change to SLI - E version.

(2009/07/08)

P.3 (MCP)Delete iGPU, Leave FDI BUS NC.
P.3 (MCP)Delete iGPU, Tied the FDI_SYNC lKohm to GND.
P.3 (MCP)Delete iGPU, Set the FDI_INT lKohm to GND.
P.4 (MCP)Delete iGPU, Set U67, A17/A18 pin to GND.
P.7 (MCP)Delete iGPU, Set VAXG to GND.
P.7 (MCP)Delete iGPU, Set SENSE and Graphice VIDs as NC.
P.9 (MCP)Support M1/M3 Path for Common Motherboard Deisgn and Stuff RP83.
P.11 (PCH)Change R902/R903 PH Power Rail to ALW.
P.11 (PCH)Delete the Dummy parts and short 0ohm. Change the U69, Pin C8/H14 Net name.
P.12 (PCH)Delete iGPU, Leave FDI BUS NC.
P.13 (PCH)Delete iGPU, Leave LVDS/CRT/DDI BUS NC.
P.14 (PCH)Change R308 from 22.6ohm to 20ohm to fix the USB Eye Diagram Issue.(BIOS: Long Topology)
P.16 (PCH)Delete iGPU, Delete CA_Dummy Parts.
P.17 (PCH)Delete iGPU, Delete CA_Dummy Parts.
P.17 (PCH)Delete iGPU, LVDS I/F Short to GND.
P.20 (DDR3)Support M1/M3 Common Motherboard Design
P.21 (DDR3)Support M1/M3 Common Motherboard Design
P.26 (ExpressCard)Short 0ohm for C/D.
P.27 (WLAN)Dummy R1560.
P.34 (CardReader) CN36 ,Change Damping value to fix the OS/US issue.
P.35 (CardReader) CN29 ,Change Damping value to fix the OS/US issue.
P.37 (Felica) C152, Change from 1206 to 0805 for Placement issue.
P.38 (eDP/LVDS) As MOR request, Defined the NEW Pin-out.
P.45 (FAN) Change the FAN Pin-Out Definition.
P.45 (FAN) Drive Out the PWM by EC Directly.
P.46 (Thermal) Dummy HW Thermal Protection G709 Function.
P.46 (Thermal) Change the U26,Pin6 Net name.
P.51 (VTT&PCH Power) Change OCP setting adjust PR113 to 56Kohm.
P.52 (DDR3 Power) Aovid the Sequence concern, from Sus rail to ALW.
P.54 (CPU VHCORE) Reserved CAP30/31 for Power Solution.
P.54 (CPU VHCORE) PR555,PR557 Compensation Adjustments.
P.54 (CPU VHCORE) PR569,PR575 Compensation Adjustments.
P.55 (CPU VID) Follow the ARD/CPD EDS Setting to set as SV type.
P.56 (VGFX Power) Delete iGPU, Delete Dummy Parts.
P.57 (VGAPower) Change OCP setting adjust PR566 to 56Kohm.
P.57 (VGAPower) PR222, PR229 Feedback Loop Adjustment
P.59 (OVP) Dummy the PWRLIMIT HW Control , Used the SW Monitor Proposal
P.60 (INV) Delete iGPU, Delete Dummy Parts.
P.61 (LVDS) Delete iGPU, Delete Dummy Parts.
P.62 (HDMI) Delete iGPU, Delete Dummy Parts.
P.63 (CRT) Delete iGPU, Delete Dummy Parts.
P.64 (Audio) Change U126 from OR gate to AND gate.
P.69 (T-JET) Add C5127 Cap.
P.74 (VGA) Change to NC, when support eDP stuffed.
P.74 (VGA) Short 0ohm , R2319,R2320 Change Net name.
P.85 (LID) Change U21 to EC2648-B3-G.

(2009/07/09)

P.26 (Expresscard)Revise the CN10 Footprint symbol for Screw PAD.
P.29 (LAN)Change the C988, C989 CL value to 12P.
P.87 (BOSS)Revise BOSS5 Footprint Symbol
P.35 (CardReader) U22 Change to 0553E1P11U.
P.34 (CardReader) Change C785/C786 value to 24P depends on Cystal report.

(2009/07/13)

P.4 (MCP)Change U67 Socket to 988A(P298827-364A-01P)
P.54 (CPU VHCORE) PR598 Loadline Fine Tune.
P.54 (CPU VHCORE) Add TP377 for L6 Power Test Usage.
P.89 (USB) Change A_CN2/A_CN3 to UB1112C-RA202-7H.
P.28 (TV) CN16 change to GB12501-10510-7H
P.87 (BOSS) Change BOSS3/BOSS4 P/N as ME request.
P.66 (Audio) Add Test Point TP379.
P.64 (Audio) Add Test Point TP327 ,TP378 ,TP380.
P.60 (INV)Iopins (CN40) and 6 Pins (CN5) Inverter Connector Co-Lay for eDP support.
P.57 (VGAPower) Add the TP221/TP248.

(2009/07/15)

P.10 (PCH)Change U98 to MX25L3205DM2I-12G.
P.61 (LVDS) Delete U46 to fix the DISPLAY OFF function issue.
P.61 (LVDS) Change R136 from 100Kohm to 10Kohm.
P.24 (SPI) U23 change to MX25L1005CMI-12G.

(2009/07/17)

P.91 (Audio) A_C25/A_C30 change from 2.2uF to 4.7uF to fix crosstalk issue.
P.59 (OVP) PR167 change to 26.1Kohm, PR169 change to 80.6Kohm ,PR171 change to 18.2Kohm for OVP Adjust.
P.54 (CPU VHCORE)PR565 change to 1.8Kohm, PC566 change to 0.022uF for IMON Adjust.
P.87 (HOLE)Revise M_H3 as ME design change.
P.87 (HOLE)Add M_PAD4 as ME request.
P.29 (LAN) Change the Y6 to 25MHZ_12P_30PPM.
P.23 (EC)C26/C27 change to 18pF.

(2009/07/23)

P.91 (Audio) Change R342 PH Power Plane to avoid Q90 abnormal behavior.
P.17 (PCH) VSSA_LVDS leave NC.
P.26 (ExpressCard) Add R345 for MOR request. (Reserve)

(2009/07/24)

P.4 (MCP)Change R1261 to Stuff as MOR request.
P.4 (MCP)INTEL S3 Power Reduction Solution Implement.
P.7 (MCP)INTEL S3 Power Reduction Solution Implement.
P.9 (MCP)INTEL S3 Power Reduction Solution Implement.
P.15 (PCH)INTEL S3 Power Reduction Solution Implement.
P.49 (Discharge) INTEL S3 Power Reduction Solution Implement.
P.52 (DDR3 Power) INTEL S3 Power Reduction Solution Implement.
P.12 (PCH)Change R911 to 10Kohm as MOR request.
P.4 (MCP)RP81, RP82 change to Array for C/D.
P.26 (ExpressCard)Short R677,R683,R682,R685 0ohm for C/D.

(2009/07/27)

P.12 (PCH)Dummy the R921 for ME function support and avoid the leakge concern.

(2009/07/28)

P.79 (VRAM) U207 ,Data Pin Swap
P.80 (VRAM) U208 ,Data Pin Swap
P.81 (VRAM) U211 ,Data Pin Swap
P.82 (VRAM) U212 ,Data Pin Swap
P.15 (PCH)RP90, RP95 ,RP96 for Reduce BOM Q'ty.
P.10 (PCH)RP93, RP94 for Reduce BOM Q'ty.
P.20 (DDR3)RP91 for Reduce BOM Q'ty.
P.23 (EC)RP92 for Reduce BOM Q'ty.
P.86 (Identify IC)PR125 for Reduce BOM Q'ty.
P.12 (PCH)Reserve R930 for Leakage Check.
P.7 (MCP)INTEL S3 Power Reduction Solution Implement Revised.
P.49 (Discharge) INTEL S3 Power Reduction Solution Implement Revised.

(2009/07/29)

P.35 (CardReader) Change R391 to 100K as VEDS.
P.27 (WLAN)Short R20.
P.49 (Discharge) INTEL S3 Power Reduction Solution Implement Revised.
P.51 (VTT&PCH Power) Change PR123 to 1Kohm
P.51 (VTT&PCH Power) Change PR160 to 1Kohm (NC)
P.57 (VGAPower) Change PR176 to 1Kohm (NC)
P.20 (DDR3) INTEL S3 Power Reduction Solution Implement Revised.
P.21 (DDR3) INTEL S3 Power Reduction Solution Implement Revised.

(2009/07/30)

P.51 (VTT&PCH Power) Change PR44 to 2.2ohm.
P.52 (DDR3 Power) Add PR41 and PC42 for PWM Setting.
P.57 (VGAPower) PR70 Change to 2.2ohm for PWM setting.
P.57 (VGAPower) Add PR163 and PC133 for PWM Setting.
P.54 (CPU VHCORE) Change PR597 to 16.5Kohm for IMON Fine Tune.
P.48 (DCIN&CHARGER) Delete PR657.

(2009/07/31)

P.12 (PCH)Add Q7 as MOR request.

(2009/08/03)

P.09 (MCP) Stuff R1582.
P.27 (WLAN)Reserve R22 for MOR request.
P.74 (VGA) Revise the Strap Pin value as FAEprovided for DVT Sample.
- N11P-GE1 x0A29
- N11M-GE1 x0A75
P.53 (+1.8V SYSPower)Fine tune RC (PR585/PC250) const. foF NVVDD Sequence Request.
P.64 (Audio) Reserve the ALC275/ALC269 BOM Mount Option.
P.57 (VGAPower) Set the P-state for N11P-GE1/N11M-GE1 QS Sample Requirement.
P.53 (+1.8V SYSPower)Change PR587 set the Vo value.
P.58 (Other Power)Change PQ44/PQ50 to IRF8736PBF.

(2009/08/04) - Pre-BOM 0.80

P.60 (INV) Delete R687 and R684 as MOR request.
P.76 (VGA) Add Test Point for eDP.
P.76 (VGA) Change R2330/R2331 for C/D thermal sensor.(DVT Verify)
P.75 (VGA) Delete Q72 as MOR request.
P.14 (PCH) Remove Braidwood (Intel Updated and MOR confirmed)
P.33 (Braidwood) Remove Braidwood (Intel Updated and MOR confirmed)

(2009/08/05)

P.76 (VGA) Stuff R5705 as FAE Request.
P.35 (CardReader)Dummy C767 and Change R1465 to 33ohm.
P.48 (DCIN&CHARGER) Add EC6~9 for EMI Solution.
P.29 (LAN) Add EC10~16 for EMI Solution.
P.88 (DB Connector) Add A_EC1~3 for EMI Solution.
P.91 (Audio) Add A_D5 for EMI Solution.
P.48 (DCIN&CHARGER) Change PQ32 EMI Solution.

(2009/08/10)

P.30 (LAN) Change the L70 to NS692412 to improve EMI.
P.64 (Audio)Add EC17 and EC19 ,EC21,EC22 for EMI Solution.
P.64 (Audio) Change R5782 to 100kohm to decrease and BEEP sound level as MOR request.
P.64 (Audio) Dummy U217 and C6063 for C/D as MOR request.
P.64 (Audio) Reserve the R5934 for C/D as MOR request.
P.64 (Audio) Delete the U215 SMB Connection.
P.65 (Audio) Add the comment for " If use ALC269 Codec, these parts should be Mount."
P.68 (Audio) Reserve the L-ch parts and add R5936 for C/D as MOR request.
P.85 (USB) C714 Change to X5R to match VEVs/VEDS requirement.
P.26 (ExpressCard)Add R636 for MOR request. (Reserve)
P.39 (BT) As MOR request, Stuff the R7 Path.
P.39 (BT)As MOR request, Add R5939 for Clock.

(2009/08/12)

P.4 (MCP)Stuff R5926 to avoid the Q73 Floating.
P.7 (MCP) Add R1561 0ohm and change C6080 to 0.01uF as INTEL update.
P.7 (MCP)INTEL White Paper0.9 Check List Request of Q55.
P.15 (PCH)Add R934 ,Follow INTEL S3 Check List 0.9. (GPO)
P.52 (DDR3 Power) Change FR39 for PWM Setting.
P.58 (Other Power)Dummy PQ44 to IRF8736PBF.
P.29 (LAN) Change the Y6 to E5FA25.0000F1D233.